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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: P60D1-US

First Inventor: Benjamin N. Eldridge et al.

Title: SPECIAL CONTACT POINTS FOR ACCESSING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT

Express Mail Label No. EE412508842US

UTILITY PATENT APPLICATION TRANSMITTAL

Box: PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

Sir:

1. X This is a request for filing a
   - _ Original
   - _ Continuation
   - X Divisional
   - _ Continuation-in-part

   application under 37 C.F.R. 1.53(b), in the name(s) of

   Benjamin N. Eldridge,
   Igor Y. Khandros,
   David V. Pedersen, and
   Ralph G. Whitten

   for

   SPECIAL CONTACT POINTS FOR ACCESSING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT.

2. X This application claims priority under 35 U.S.C. 120 to pending application Serial No. 09/224,169, filed December 31, 1998, which is currently pending in Group Art Unit 2858 before Examiner Jimmy Nguyen.

   X Please amend the specification by inserting before the first line the sentence:

   --This is

   - _ a continuation
   - X a divisional
   - _ a continuation-in-part

   application of Serial No. 09/224,169, filed December 31, 1998.—

   X Prior application Serial No. 09/224,169, filed December 31, 1998, is hereby incorporated herein by reference.

X

3. X Enclosed are the following application elements:

___ New a new specification (total pages _) and new drawings (total sheets _).

X A copy of the prior specification (total pages 42) and the prior drawings (total sheets 19).

___ A new Declaration and Power of Attorney.

X A copy of the prior Declaration as originally filed.

___ A signed statement deleting inventor(s).

___ A communication regarding the post office address(es) of the inventor(s).

4. X The filing fee is calculated below:

Claims as filed in the prior application, less any claims canceled by amendment below, plus any claims added by preliminary amendment:

	(Col. 1) NO. FILED	(Col. 2) NO. EXTRA	SMALL ENTITY RATE	FEE	OTHER THAN SMALL ENTITY RATE	FEE
BASIC FEE				$355		**$710**
TOTAL CLAIMS	34 - 20 =	14	x 9 =	$	x 18 =	$252
INDEP CLAIMS	3 - 3 =	0	x 40 =	$	x 80 =	$0
MULTIPLE DEPENDENT CLAIM PRESENTED			+135 =	$	+270 =	$0
If the difference in Col 1 is less than zero, enter "0" in Col. 2			TOTAL	$	TOTAL	**$962**

5. X The Commissioner is hereby authorized to charge the above filing fee of $962 and any additional fees which may be required, including extension fees, or credit any overpayment to Deposit Account No. 50-0285 (Order No. P60D1-US).

___ Our check in the amount of $_____ is enclosed.

6. X Cancel in this application original claims 35-64 of the prior application before calculating the filing fee.

7. ___ Priority of application Serial No. _____ filed on _____ in _____ is claimed under 35 U.S.C. 119.

___ The certified copy has been filed in prior application Serial No. _____ filed on _____.

8. X The prior application is assigned of record to FormFactor, Inc., a Delaware corporation.

9. X The power of attorney as originally filed in the prior application has

___ not changed, and

___ the power appears in the original papers in the prior application

___ a copy of the power in the prior application is enclosed.

_X_ changed, and

_X_ a copy of the most recent power in the prior application is enclosed.

___ a new power has been executed and is enclosed.

10. X The correspondence address

___ has not changed and is:

_X_ has been changed to:

FormFactor, Inc.
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Telephone: 925-294-4300
Fax: 925-294-8147

11. ___ A preliminary amendment is enclosed.

12. ___ An Information Disclosure Statement Is enclosed.

Date: December 29, 2000

Signature: _____
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Express mail no. EE412508842US.
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42 pages of specification.
19 Sheets of drawings.

UNITED STATES PATENT APPLICATION

FOR

SPECIAL CONTACT POINTS FOR ACCESSING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT

SPECIAL CONTACT POINTS FOR ACCESSING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The present invention relates to integrated circuit (IC) semiconductor devices and, more particularly, to testing the devices.

BACKGROUND

Large numbers of identical integrated circuits such as microprocessors, memory devices, and digital signal processing devices are generally fabricated on a silicon wafer. Due to defects that may occur during fabrication, each IC (die) on the wafer is typically tested or sorted by test equipment such as automatic test equipment (ATE) machines and probe cards. The test signals are provided to each die through input or input/output (I/O) bond pads on each die, and the test results are monitored on output or I/O bond pads. The good die that pass the wafer-level test are then singulated and packaged typically by electrically connecting the bond pads to the package by means of bond wires, solder balls, or other contact structures. To accommodate the bonding wires or solder balls, the bond pads are generally very large relative to the circuit elements of the integrated circuit. Typical bond pad sizes are on the order of 100 μm (microns) x 100 μm (4 mils X 4 mils). The bond pads are also typically aligned in regular patterns such as peripherally along the outside perimeter of the die, in a grid pattern, or in a column or row generally through the center of the die (lead-on-center).

The bond pads allow each die as a whole to be functionally tested for specified timing parameters (AC parameters), DC parameters, and overall operation. The bonding pads may also be used to load test patterns and monitor test result from on-chip test circuits such as SCAN circuitry and Built-In Self-Test (BIST) circuitry. The on-chip test circuits enhance the

overall testing of a die by enabling individual testing of internal circuits or nodes. However, this comes at the expense of increasing the size of the die to accommodate the added test circuitry and additional bond pads needed to support the on-chip test circuitry.

If a die already has all of its peripheral, grid, or lead-on-center bond pad locations dedicated to a device function, then adding additional bond pads in the predetermined bond pad alignment to support the on-chip testing circuitry can result in a substantial increase in the size of the die. Generally, larger die are more prone to defects and consequently more expensive to manufacture. Additionally, on-chip testing circuitry can result in a significant increase in test time as many clock cycles may be required to load test input data and subsequently output test results from a few available bond pads. On-chip testing circuitry also does not allow for direct external access to internal circuit nodes. Test input data and test results must pass through the SCAN circuitry or BIST circuitry before it can be monitored. This introduces additional circuits that can mask failures in the circuit intended to be tested, or can introduce new failures caused by SCAN or BIST circuitry.

Additionally, many designs are I/O limited since only a limited number of leads (e.g., bond wires) may be accommodated in a given packaging scheme. Moreover, to test I/O functionality of a chip, these same lead locations must be used. It would be advantageous to access more points in a circuit, especially for testing. It would also be advantageous if the access points could be located with a high degree of positional freedom. Small size, large number, and arbitrary or selected positioning of the access points would also be advantageous.

SUMMARY OF THE INVENTION

One embodiment of the present invention concerns an integrated circuit that includes bond pads and special contact pads or points. The bond pads are for interfacing the integrated circuit as a whole with an external circuit, and are to be bonded to a package or circuit board. The bond pads are disposed on the die in a predetermined alignment such as a peripheral, grid, or lead-on-center alignment. The special contact pads are used to provide external test patterns to internal circuits and/or to externally monitor results from testing the internal circuits. The special contact pads may be advantageously located on the integrated circuit with a high degree of positional freedom. For one embodiment, the special contact pads may be disposed on the die at a location that is not in the same alignment as the bond pads. The special contact pads may be smaller than the bond pads so as not to increase the die size due to the special contact pads. The special contact points may also be used to externally program internal circuits (e.g., nonvolatile circuits) at the die or package level. The special contact points may also be used to select redundant circuits for faulty circuits.

Other objects, features, and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention are illustrated by way of example and are by no means intended to limit the scope of the present invention to the particular embodiments shown, and in which:

Figure 1 is a plan view of one embodiment of an integrated circuit having peripheral bond pads, internal circuitry, and special contact pads disposed about internal circuitry and for testing the internal circuitry;

Figure 2 is a plan view of one embodiment of an integrated circuit having peripheral bond pads, internal circuitry, and special contact pads collectively disposed in a separate region of the integrated circuit;

Figure 3A is a plan view of one embodiment of an integrated circuit, internal circuitry, and special contact pads disposed over the internal circuitry;

Figure 3B is a logic diagram of one embodiment of a special contact pad coupled to an internal circuit node via a bi-directional buffer;

Figure 4 is a plan view of one embodiment of an integrated circuit having bond pads aligned in a grid pattern, special contact pads not aligned in the grid pattern, and special contact pads aligned in the grid pattern;

Figure 5 is a side cross-sectional view of a special contact pads disposed between two bond pads;

Figure 6 is a plan view of one embodiment of an integrated circuit having lead-on-center bond pads, internal circuitry, and special contact pads for testing the internal circuitry;

Figure 7 is block diagram of one embodiment of sequential circuit blocks and special contact pads for testing the sequential circuits;

Figure 8 is a block diagram one embodiment of using special contact pads to isolate a faulty circuit block and enable a redundant circuit block;

Figure 9 is a circuit diagram of one embodiment of the switch of Figure 8;

Figure 10 is a block diagram of another embodiment of using special contact pads to isolate a faulty circuit block and enable a redundant circuit block;

Figure 11 is a block diagram of one embodiment of using a special contact pad to enable or stimulate a circuit under test;

Figure 12 is a block diagram of one embodiment of using a special contact pad to provide a control signal to scan circuitry;

Figure 13 is a side cross-sectional view of one embodiment of a probe card assembly having a probe card with cantilevered probes for probing bond pads and special contact pads of an integrated circuit;

Figure 14 is a plan view of the probe card of Figure 13;

Figure 15 is a side cross-sectional view of one embodiment of a probe card assembly having a membrane probe card with contacts for probing bond pads and special contact pads of an integrated circuit;

Figure 16 is a plan view of the membrane probe card of Figure 15 having contact balls aligned in a grid pattern for contacting bond pads, and having contact balls not aligned in the grid pattern for contacting special contact pads;

Figure 17 is a plan view of the membrane probe card of Figure 15 having contact balls aligned in a peripheral pattern for contacting bond pads, and having contact balls not aligned in the peripheral pattern for contacting special contact pads;

Figure 18 is a side cross-sectional view of another embodiment of a probe card assembly having a COBRA-style probe card assembly with probes for probing bond pads and special contact pads of an integrated circuit;

Figure 19 is a plan view of the COBRA-style probe tips of Figure 18 having some tips aligned in a grid pattern to contact bond pads, and having other tips not aligned in the grid pattern to contact special contact pads;

Figure 20 is a plan view of the COBRA-style probe tips of Figure 18 having some tips aligned in a peripheral pattern to contact bond pads, and having other tips not aligned in the peripheral pattern to contact special contact pads;

Figure 21 is a side cross-sectional view of one embodiment of a probe card assembly having spring contact elements for probing bond pads and special contact pads of an integrated circuit;

Figure 22 is another embodiment of the probe card assembly of Figure 21 in which the spring contact elements, the bond pads, and the special contact pads have varying heights;

Figure 23 is another embodiment of the probe card assembly of Figure 21 in which the spring contact elements are disposed on the integrated circuit;

Figure 24 is a side cross-sectional view of one embodiment of a spring contact element of Figure 21;

Figure 25 is a perspective view of one embodiment of the contact tip structure and pyramid-shaped contact feature of the spring contact element of Figure 21;

Figure 26 is a perspective view of one embodiment of the pyramid-shaped contact tip structure of Figure 25;

Figure 27 is a side cross-sectional view of another embodiment for performing wafer-level test of an integrated circuit having bond pads and special contact pads;

Figure 28 is a side cross-sectional view of one embodiment of a socket for retaining a package having special contact points and conventional input, output, and input/output pins;

Figure 29A is a side cross-sectional view of another embodiment of a spring contact element;

Figure 29B is a perspective view of the spring contact element of Figure 29A;

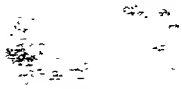
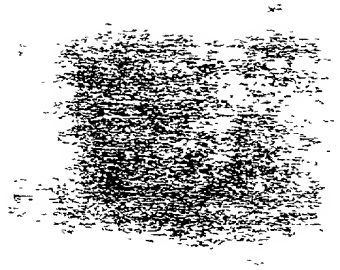


Figure 30A is a perspective view of another embodiment of a spring contact element;

Figure 30B is a side cross-sectional view of the spring contact element of Figure 30A; and

Figure 31 is a perspective view of another embodiment of a tip structure for a spring contact element.



DETAILED DESCRIPTION

Figure 1 shows an integrated circuit or die 100 that includes bond pads 110, special contact pads 112, and internal circuits 102, 104, 106 and 108. Internal circuits 102-106 may be any circuit blocks such as memory, control logic, programmable logic, and the like. Bond pads 110 are conventional input, output, or I/O pads for electrically interfacing internal circuits 102-108 with circuits external to integrated circuit 100. Bond pads 110 are peripherally disposed about the perimeter of integrated circuit 100, and are typically large enough to accommodate a probe tip of a probe of wafer sort probe card, a bond wire, or a solder ball.

Special contact pads 112 provide a means for providing test input data to, and monitor signals from, internal circuits 102-106 without having to test the function of the entire integrated circuit. Special contact pads 112 also provide a means for testing internal circuits 102-106 when these circuits are not otherwise individually testable and/or accessible through bond pads 110. For one example, internal circuit 102 may be an embedded memory that is not directly accessible through bond pads 110. Address and input data signals may be provided over several of the special contact pads 112 to provide test patterns to the embedded memory, and another group of special contact pads 112 may receive data read from the memory. The external circuitry providing the test patterns for the embedded memory may provide any number of patterns to increase the fault coverage.

For another embodiment, internal circuit 102 may be a programmable circuit such as nonvolatile memory or programmable logic. Data can be programmed into the internal circuit through the special contact pads 112. For example, BIOS information, program code, and system software may be programmed or updated in programmable circuit 102 after fabrication of integrated circuit 100.

On-chip test circuitry such as SCAN and BIST circuitry may not be required in integrated circuit 100 as test stimuli for integrated circuits 102-106 may be provided directly to special contact pads 112. Additionally, test results may be output to special contact pads 112 rather than bond pads 110. The external test circuitry supplying the test stimuli may provide an increased number of tests without impacting the size of integrated circuit 100. Without SCAN or BIST circuitry included in a test input or output signal path, the likelihood of more accurately determining the location of a failure increases as there is no on-chip test circuitry to mask the failure or to introduce further failures. Additionally, speed parameters or the timing of signals into and out of a circuit block or a circuit node may be more accurately measured and monitored without introducing delays caused by intermediary on-chip test circuitry.

As shown in integrated circuit 100, special contact pads 112 may also work with BIST circuitry 108 (or other on-chip test circuitry) to monitor the response of internal circuit 106 to test stimuli provided by BIST 108. This can be accomplished without having to add additional bond pads 110, or to use existing bond pads 110 to communicate with BIST 108.

As shown in Figure 1, special contact pads 112 are disposed within a region surrounded by peripheral bond pads 110. As special contact pads 112 are not disposed in the predetermined peripheral alignment of bond pads 110, the size of integrated circuit 100 may not be increased by adding special contact pads 112. For other embodiments, the number and placement of special contact pads 112 may increase the size of integrated circuit 100.

Special contact pads 112 may also be interspersed between bond pads 110 (e.g., see Figure 5), or be located outside the region surrounded by bond pads 110. For one embodiment in which special contact pads 112 are interspersed between bond pads 110, it may be advantageous for special

contact pads 112 to be smaller than bond pads 110 so as not to increase the size of integrated circuit 100.

Special contact pads 112 may be any size including sizes smaller than bond pads 110. When special contacts 112 are smaller than bond pads 110, more special test pads may be disposed on integrated circuit 100 without increasing the size of the die over that defined by the peripheral bond pads 110. A larger number of special contact pads may increase the number and/or complexity of tests that can be provided to the internal circuit, and thus may increase the fault coverage and robustness of tests. For one embodiment, a bond pad 110 may be approximately 100 μm X 100 μm, and a special contact pad may be approximately 5 to 10 μm per side. In other embodiments, the special contact pad may be less than 5 μm per side. For still other embodiments, the special contact pads may be manufactured to have different sizes to accommodate their different spatial locations on the die (e.g., between bond pads 110 vs. within the area surrounded by bond pads 110), to accommodate different dimensions of various probe tips, bond wires, or solder balls, or to accommodate different functions of the circuits under test (i.e., nodes driving output signals may required larger pads than pads for providing input signals, or vice versa). The lower limit for the size of the special contact pads may be limited by the accuracy of the probe-to-pad alignment and the size of the probe.

Special contact pads 112 may be formed into an approximately square shape, rectangular shape, or any other geometric shape. Special contact pad 112 may also have different heights than bond pads 110. Special contacts pads 112 may be fabricated using conventional photolithography processes that are typically used to create bond pads or other, relatively flat, conductive landings. For one embodiment, the special contact pads may be fabricated

from one or more metal layers including aluminum, copper, gold, or other metals or conductive materials.

Integrated circuit 100 shows that special contact pads 112 are logically disposed about the circuit block which they test. In alternative embodiments, special contact pads 112 may be physically located at any other location in integrated circuit 100. Figure 2 shows that special contact pads 112 need not be logically disposed about internal circuits 102 and 106, but may be physically located in region 202. For alternative embodiments, the special contact pads 112 may be located in any area of integrated circuit 100.

Figures 1 and 2 show that special contact pads 112 may be used to test or monitor signals from an internal circuit block. Figure 3A shows that the special contact pads may also be disposed directly over internal circuits 102-106 to monitor or excite a particular circuit node within an internal circuit block. For example, a speed critical path within an embedded memory block or other circuit may be monitored. Alternatively, the voltage level on an internal circuit node or of an internally generated reference voltage source may be monitored.

Special contact pads 112 may not be permanently bonded out to a integrated circuit package (e.g., typical plastic and ceramic chip packages), rather, the special contact pads may be used for receiving test input information (e.g., address, control, or data) or monitoring internal test nodes or signals. The special contact pads are large enough, however, to receive an electrical contact element (as will be described in more detail below). Given that special contact pads 112 are generally not bonded out to a package, special contacts pads 112 may require significantly less supporting circuitry than is typically required by bond pads 110. Typical bond pads generally include supporting circuitry that requires significant amounts of silicon die are. Examples of supporting circuitry include electrostatic-discharge (*ESD*)

protection structures such as resistors, capacitors, and/or diodes, latch-up prevention circuits such as guard rings, buffers for driving circuits and signal lines external to the integrated device or for buffering internal signals received from external signal lines, logic or voltage translation circuits, and noise reduction circuitry. Special contact pads 112 may reduce the amount of supporting circuitry required. Little no ESD protection may be needed and little or no buffering may be required for an external probe to electrically contact a special contact pad and monitor a signal thereon. For one example, an I/O buffer 120 may be used between an internal test point 124 and a special contact pad 110 as shown in Figure 3B. The I/O buffer may be controlled by a control signal 122. The I/O buffer 120 may be approximately 10 to 100 times weaker than that required for a bond pad having to drive heavy loads in a PCB environment. Additionally, little or no latch-up supporting circuitry or noise reduction circuitry may be required. For example, a weak pull-up resistor may be all that is required for each special contact pad for noise reduction circuitry. Generally, a special contact pad may require only 1 to 50 percent of the supporting circuitry typically required for a bond pad.

Figure 4 shows an integrated circuit 400 that includes bond pads 410 aligned in a Land Grid Array (LGA) pattern for bonding to contact balls (e.g., solder or other metal interconnect) in a control collapse chip connection (C4) or flip-chip arrangement. Selectively dispersed within and outside of the grid pattern are special contact pads 412 that, as in Figures 1-3, may be used to provide test signals to or monitor signals from internal circuits of integrated circuit 400. In this embodiment, special contact pads 412 may be smaller than the bond pads or contact balls so as not to increase the size of integrated circuit 400 over the minimum size required for a given number of bond pads 410. In alternative embodiments, the special contact pads 412 may be the same size as bond pads 410.

Figure 5 shows a side cross-sectional view of a special contact pad 412 disposed between two bond pads 410. Bond pads 410 have contact balls 504 formed thereon, and are typically spaced with a minimum pitch 502 between their centers of approximately 10 mils (0.010") or 250 μm. The minimum diameter 508 of the contact balls 504 is typically on the order of the 1 to 3 mils, and the minimum distance 506 between the edges of contact balls 504 is typically on the order of 7 to 9 mils. Special contact pad 412 can be sized to fit between bond pads 410, and may have a width 510 of less than 9 mils. For other embodiments, special contact pad 412 may have a width of approximately 1 to 5 mils. For still other embodiments, special contact pad 412 may have a width of less than 1 mil. Special contact pad 412 may be formed into an approximately square shape, rectangular shape, or any other geometric shape. Special contact pad 412 may also have a height different than that of bond pads 410.

For an alternative embodiment, contact balls 504 need not be formed on bond pads 410.

The embodiments shown in Figures 4 and 5 may also be a LGA package such as Ball Grid Array (BGA) package, Pin Grid Array (PGA) package, C4 package, or flip chip package that has pins or contact balls 410 for interfacing with a socket or printed circuit board (PCB). Special contact pads 412 may be additional pins or pads that can receive test signals or provide test output signals or other signals to probes, a socket, or PCB.

Figure 5 also illustrates a special contact pad 412 disposed between two bond pads 410 arranged in a peripheral alignment (as shown in Figure 1).

Figure 6 shows an integrated circuit 600 that includes bond pads 610 arranged as a column (or row) in a lead-on-center pattern. Selectively dispersed within and outside of the lead-on-center pattern are special contact

pads 612 that, as in Figures 1-5, may be used to provide test signals to or monitor signals from internal circuits 602 and 604 of integrated circuit 600.

Figures 1-6 show that internal circuit blocks or circuit nodes can be tested or monitored by special contact pads. Figure 7 shows that sequential internal circuit blocks 702, 704, and 706 can also be tested by special contact pads with or without the use of bond pads. In this embodiment, test input data is provided on special contact pads 712 to an embedded memory 702. For an alternative embodiment, the input data can be provided from bond pads. The test data may include an address, control signals (e.g., read, write, etc.), and/or a test pattern. Assuming that the test data is an address of a location within memory 702, data stored at the accessed address may be provided to I/O interface 704 and monitored by special contact pads 713. The access time (i.e., address to data out) of memory 702 may be more accurately measured by special contact pads 712 and 713 as no additional time is introduced due to circuit blocks such as I/O interface 704 and I/O drivers 706. Conventional approaches of using BIST circuitry would typically include additional on-chip circuitry to provide address signals, for example, to memory 702, and then external circuitry could monitor the results at one or more of bond pads 716. This conventional approach, however, would be unable to monitor the outputs of memory 702 directly (as with special contact pads 713) and thus would not be able to directly measure the actual access time of memory 702.

In response to the data read from memory 702, I/O interface 704 may format the data prior to providing it to I/O drivers 706. I/O interface 704 may receive control signals on special contact pads 714, or internal circuit nodes within I/O interface 704 may be monitored by special contact pads 714. The data output by I/O interface 704 to I/O drivers 706 may be monitored via special contact pads 715. I/O drivers 706 may then drive the data to bond pads 716.

Since special contact pads 713 and 715 and bond pads 716 may be used to monitor the output of each of memory 702, I/O interface 704, and I/O divers 706, respectively, such that incorrect data received at bond pads 716 can be isolated to the circuit which caused the failure. In conventional BIST techniques in which an address, for example, is provided to memory 702, the source of incorrect data received at bond pads 716 would be unknown.

While the embodiment shown in Figure 7 includes a specific example of accessing data in an embedded memory 702, the example also applies to introducing and monitoring signals from a series of any other circuit blocks.

Special contact pads may also be used to not only isolate failures, but to also enable redundant circuits to be used to replace faulty circuits. Figure 8 shows one embodiment of using special contact pads to identify faulty circuit blocks and enable a redundant circuit to replace the faulty circuit block. This embodiment again uses the example of accessing data in an embedded memory, but can be extended to a series of circuits in which one of the circuits has a redundant circuit.

Figure 8 includes a redundant I/O interface 705 that can replace a defective I/O interface 704. The outputs of memory 702 are provide to both of I/O interfaces 704 and 705. The outputs of I/O interface 704 can be monitored through special contact pads 715, and the outputs of redundant I/O interface 705 can be monitored through special contact pads 717. If the outputs of I/O interface 704 are as expected indicating that I/O interface 704 is operating correctly, multiplexer 708 is configured by the control signal on line 721 to allow the signals on lines 723 to be provided to I/O drivers 706. If, however, the outputs of I/O interface 704 are not as expected indicating that I/O interface 704 is malfunctioning, and the outputs of redundant I/O interface 705 are as expected, then multiplexer 708 is configured by the control signal on line 721 to allow the signals on lines 725 to be provided to I/O drivers 706.

The signals output by multiplexer 708 may be monitored via special contact pads 719.

The control signal on line 721 can be driven to the appropriate voltage level or logic state by switch 710. In response to a TOGGLE signal, either voltage V1 or V2 will be selected in response to monitoring the signals at the special contact pads 717 and 715. The TOGGLE signal can be controlled by another special contact pad (not shown).

Figure 9 shows switch 910 that is one embodiment of switch 710 of Figure 7. Other embodiments of switch 710 may also be used. Switch 910 includes a PMOS transistor biased into an on-state by having its gate coupled to ground, its source coupled to a power supply VDD, and its drain coupled to signal line 721. Switch 910 also includes a fuse element 904 that is coupled between signal line 721 and ground. The fuse element may be a metal fuse, resistive fuse, or memory element. When fuse 904 is blown in response to the TOGGLE signal, signal line 721 is pulled towards VDD and the signals on lines 725, for example, are output by multiplexer 708. When fuse 904 is not blown, signal line 721 is pulled towards to ground by fuse 904 and the signals on lines 723, for example, are output by multiplexer 708. Fuse 904 may be blown using several well-known techniques including using a laser pulse or electrical currents. For one embodiment, a special test pad may be used to provide an electrical current that blows fuse 904.

Figure 10 shows an alternative embodiment of the redundancy scheme of Figure 8. In Figure 10, groups of fuses 1002, 1004, 1006, and 1008 may be included before and after the I/O interfaces. When one of the I/O interface is identified as defective it may be isolated by an appropriate fuse group. For example, if I/O interface 704 is defective and I/O interface 705 is functioning correctly, then fuse groups 1004 and 1008 may be blown so as to isolate I/O interface 704. The fuse groups 1004 and 1008 may be blown via special contact

pads (not shown) that provide one or more signals that cause a large amount of current to flow through fuse groups 1004 and 1008. Alternative means to blow the fuses may also be used.

As discussed above with respect to Figure 1, special contact pads can be used together with on-chip test circuitry to test an integrated circuit. Figure 11 shows one embodiment in which one (or more) special contact pad 1110 is used to provide a clock signal, reset signal, enable signal, or other control signal to BIST 1102. In response, BIST 1102 provides one or more test signals to internal circuit 1104 and/or internal circuit 1106. The results of the internal test may then be monitored at bond pads 1108 (or alternatively at other special contact pads). For other embodiments, a special contact pad may also be used to provide an enable signal or a clock signal to any other internal circuit.

Similarly, as shown in Figure 12, one (or more) special contact pad 1210 may be used to provide a clock signal, reset signal, enable signal, or other control signal to shift register elements 1206 and 1208 of a SCAN circuit. The SCAN circuit may be coupled between bond pads 1212 and 1214 (or, alternatively, one or more special contact pads) that may receive SCAN input data (SI), and provide SCAN output data (SO), respectively.

For an alternative embodiment, one or both of pads 1212 may be special contact pads. This may provide for increased design flexibility in the location and use of SCAN circuitry. For example, this may enable multiple SCAN regions or circuits of varying size and complexity to test various different internal circuits or blocks of circuits.

When the special contact pads are available on a die of a wafer, test signals may be supplied to special contact pads, or signals may be monitored at the special contact pads by means of test or probe card assemblies. Probe card assemblies typically include a probe card that has a number of probe elements

or contact structures to contact the special contact pads and bond pads. A host controller or other logic device typically communicates with the integrated circuit under test through the probe card.

Figure 13 illustrates one embodiment of an test system 1300 for performing a wafer-level sort test of a die 1311 that includes bond pads 1314 and special contact pads 1316. Die 1311 is formed on wafer 1312 that may be disposed on a suitable support structure such as a vacuum chuck (not shown). Die 1311 may embody an integrated circuit such as integrated circuit 100 of Figure 1.

System 1300 includes a test head 1304 and a probe card assembly 1313. Probe card assembly 1313 includes a load board or interconnection substrate 1306 and cantilevered or needle probe card 1310. Host 1302 communicates test signals with test head 1304. Any type of host may be used including a personal computer, or specialized machines such as Automatic Test Equipment (ATE) provided by LTX, Credence, Teradyne, and others. Test head 1304 typically includes drivers, receivers, and parametric measuring units (PMUs) that communicate signals with load board 1306 and probe card 1310. Load board 1306 is typically a PCB that provides the appropriate mechanical interconnection and load circuits for probe card 1310. In alternative embodiments, load board 1310 may be omitted. Load board 1310 may also include control logic such as logic 1308. Control logic 1308 may be an application-specific IC (ASIC) used to provide tests to die 1311 under the control of host 1302.

Probe card 1310 is a cantilevered or needle probe card that includes cantilevered probes 1318 and 1320 that provide signals to and receive signals from die 1311. Probes 1318 and 1320 may comprise any suitable conductive material including tungsten. As shown in the plan view of probe card 1310 in

Figure 14, probes 1318 and 1320 are connected to contact pins or points 1322 that contact load board 1306 or test head 1304.

Probes 1318 are provided in a predetermined alignment to contact bond pads 1314. As shown in Figure 14, probes 1318 make a relatively rectangular shape. Probes 1320 are provided to contact special contact pads 1316 of die 1311. Probes 1320 are generally not disposed in the same predetermined alignment of the probes 1318; rather, they extend into the region surrounded by probes 1318 (and bond pads 1314). In alternative embodiments, probes 1320 may exist outside of the region surrounded by probes 1318, or they may be disposed in the same predetermined alignment with probes 1318 and bond pads 1314.

In another embodiment, probes 1318 may be arranged in a lead-on-center arrangement to align with lead-on-center bond pads on a die, and probes 1320 may be arranged outside the lead-on-center arrangement to align with corresponding special contact pads.

While Figures 13 and 14 show that a single probe card and probe card assembly may be used to communicate with special contact pads 1316 and bond pads 1314, in alternative embodiments, separate probe cards may be used for probing special contact pads 1316 and bond pads 1314. That is, one or more probe cards may be used to contact only bond pads 1314 with one or more of probes 1318, and one or more additional probe cards may be used to contact special contact pads 1316 with one or more probes 1320. In still other embodiments, multiple probe cards may be used that have a mixture of probes 1318 and 1320.

For an alternative embodiment, bond pads 1316 and special contact pads 1316 may be of different heights. For example, bond pads 1314 may be taller than special contact pads 1316 (or vice versa). For this embodiment,

probes 1318 and 1320 may extend to different depths. That is, probes 1320 may extend lower than probes 1318 to make contact with special contact pads 1316.

Figure 15 illustrates test system 1500 that is another embodiment for performing a wafer-level sort test of a die 1511 that includes bond pads 1514 and special contact pads 1516. Die 1511 is formed on wafer 1512 that may be disposed on a suitable support structure such as a vacuum chuck (not shown). Die 1511 may embody an integrated circuit such as those described with respect to Figures 1-6.

System 1500 includes a test head 1504 and a probe card assembly 1513. Probe card assembly 1513 includes a load board or interconnection substrate 1506 and membrane probe card 1510. Like host 1302 of Figure 13, host 1502 communicates test signals with test head 1504. Test head 1504 typically includes drivers, receivers, and parametric measuring units (PMUs) that communicate signals with load board 1506 and probe card 1510. Load board 1506 is a PCB that typically provides the appropriate mechanical interconnection and load circuits for probe card 1510. In alternative embodiments, load board 1510 may be omitted. Load board 1510 may also include control logic such as logic 1508. Control logic 1508 may be an ASIC used to provide tests to die 1511 under the control of host 1502.

Probe card 1510 is a membrane probe card that includes contact balls 1518 and 1520 that provide signals to and receive signals from die 1511. Contact balls or probes 1518 and 1520 may comprise any suitable conductive material including solder.

Probes 1518 are provided in a predetermined alignment to contact bond pads 1514. As shown in Figure 16, probes 1518 may be arranged in a grid array to contact bond pads 1514 arranged in a corresponding grid array pattern. Probes 1520 may be aligned in the predetermined grid array, outside of the grid array pattern, or interspersed within the grid array pattern as shown in

Figure 16 to align with corresponding special contact pads 1516 on die 1511. Alternatively, as shown in Figure 17, probes 1518 may be arranged in a peripheral pattern to contact bond pads 1514 arranged on die 1511 in a corresponding peripheral pattern. Probes 1520 may be aligned in the predetermined peripheral pattern, outside of the peripheral pattern, or within the peripheral pattern as shown in Figure 17 to align with corresponding special contact pads 1516 on die 1511. In yet another embodiment, probes 1518 may be arranged in a lead-on-center arrangement to align with lead-on-center bond pads on a die, and probes 1520 may be arranged within or outside of the lead-on-center arrangement to align with corresponding special contact pads.

While Figures 15-17 show that a single probe card and probe card assembly may be used to communicate with special contact pads 1516 and bond pads 1514, in alternative embodiments, separate probe cards may be used for probing special contact pads 1516 and bond pads 1514. That is, one or more probe cards may be used to contact only bond pads 1514 with one or more of probes 1518, and one or more additional probe cards may be used to contact special contact pads 1516 with one or more probes 1520. In still other embodiments, multiple probe cards may be used that have a mixture of probes 1518 and 1520.

For an alternative embodiment, bond pads 1516 and special contact pads 1516 may be of different heights. For example, bond pads 1514 may be taller than special contact pads 1516 (or vice versa). For this embodiment, probes 1518 and 1520 may have different heights. That is, probes 1520 may extend lower than probes 1518 to make contact with special contact pads 1516.

Figure 18 illustrates test system 1800 that is another embodiment for performing a wafer-level sort test of a die 1811 that includes bond pads 1814 and special contact pads 1816. Die 1811 is formed on wafer 1812 that may be disposed on a suitable support structure such as a vacuum chuck (not shown).

Die 1811 may embody an integrated circuit such as those described with respect to Figure 1-6.

System 1800 includes a test head 1804 and a COBRA-style probe card assembly 1813. The COBRA-style probe card assembly is available from Wentworth Laboratories of Brookfield CT. The COBRA-style probe card assembly includes a load board or interconnection substrate 1806, space transformer (either wired or ceramic) 1808, and head assembly 1807. Head assembly 1807 includes upper plate 1809, spacer 1810, lower plate 1811, and COBRA-style probes 1818 and 1820. Like host 1302 of Figure 13, host 1802 communicates test signals with test head 1804. Test head 1804 typically includes drivers, receivers, and parametric measuring units (PMUs) that communicate signals with load board 1806 and probe card assembly 1813. Load board 1806 is a PCB that typically provides the appropriate mechanical interconnection and load circuits for probe card assembly 1813. In alternative embodiments, load board 1810 may be omitted. Load board 1810 may also include control logic to provide tests to die 1811 under the control of host 1802.

Probes 1818 are provided in a predetermined alignment to contact bond pads 1814. As shown in Figure 19, probes 1818 may be arranged in a grid array to contact bond pads 1814 aligned in a corresponding grid array pattern. Probes 1820 may be arranged with the predetermined grid array, outside of the grid array pattern, or interspersed within the grid array pattern as shown in Figure 19 to align with corresponding special contact pads 1816 on die 1811. Alternatively, as shown in Figure 20, probes 1818 may be arranged in a peripheral pattern to contact bond pads 1814 arranged on die 1811 in a corresponding peripheral pattern. Probes 1820 may be aligned in the predetermined peripheral pattern, outside of the peripheral pattern, or within the peripheral pattern as shown in Figure 20 to align with corresponding

special contact pads 1816 on die 1811. In yet another embodiment, probes 1818 may be arranged in a lead-on-center arrangement to align with lead-on-center bond pads on a die, and probes 1820 may be arranged within or outside of the lead-on-center arrangement to align with corresponding special contact pads.

While Figures 18-20 show that a single probe card assembly may be used to communicate with special contact pads 1816 and bond pads 1814, in alternative embodiments, separate probe card assemblies may be used for probing special contact pads 1816 and bond pads 1814. That is, one or more probe card assemblies may be used to contact only bond pads 1814 with one or more of probes 1818, and one or more additional probe card assemblies may be used to contact special contact pads 1816 with one or more probes 1820. In still other embodiments, multiple probe card assemblies may be used that have a mixture of probes 1818 and 1820.

For an alternative embodiment, bond pads 1816 and special contact pads 1816 may be of different heights. For example, bond pads 1814 may be taller than special contact pads 1816 (or vice versa). For this embodiment, probes 1818 and 1820 may extend to different depths (or have different heights). That is, probes 1820 may extend lower than probes 1818 to make contact with special contact pads 1816.

Figure 21 illustrates test system 2100 that is another embodiment for performing a wafer-level sort test of a die 2111 that includes bond pads 2114 and special contact pads 2116. Die 2111 is formed on wafer 2112 that may be disposed on a suitable support structure such as a vacuum chuck (not shown). Die 2111 may embody an integrated circuit such as those described with respect to Figures 1-6.

Apparatus 2100 includes a test head 2104 and a probe card assembly 2113 such as that provided by FormFactor, Inc. of Livermore, CA. One embodiment of probe card assembly 2113 is disclosed in U.S. patent

Application No. 08/789,147 filed on January 24, 1997, which is incorporated by reference herein. Probe card assembly 2113 generally includes probe card 2106, interposer 2108, space transformer 2108, and spring contact elements 1218 and 1220. Like host 1302 of Figure 13, host 2102 communicate test signals with test head 2104. Test head 2104 typically includes drivers, receivers, and parametric measuring units (PMUs) that communicate signals with probe card assembly 2113. Probe card assembly 2113 may also include control logic to provide tests to die 2111 under the control of host 2102.

Spring contact elements 2118 are formed in a predetermined alignment to contact bond pads 2114. Probes 2118 may be arranged in a grid array to contact bond pads 2114 aligned in a corresponding grid array pattern. Spring contact elements 2120 may be arranged with the predetermined grid array, outside of the grid array pattern, or interspersed within the grid array pattern to align with corresponding special contact pads 2116 on die 2111. Alternatively, spring contact elements 2118 may be arranged in a peripheral pattern to contact bond pads 2114 arranged on die 2111 in a corresponding peripheral pattern. Spring contact elements 2120 may be aligned in the predetermined peripheral pattern, outside of the peripheral pattern, or within the peripheral pattern to align with corresponding special contact pads 2116 on die 2111. In yet another embodiment, spring contact elements 2118 may be arranged in a lead-on-center arrangement to align with lead-on-center bond pads on a die, and spring contact elements 2120 may be arranged within or outside of the lead-on-center arrangement to align with corresponding special contact pads.

While Figure 21 shows that a single probe card assembly may be used to communicate with special contact pads 2116 and bond pads 2114, in alternative embodiments, separate probe card assemblies may be used for probing special contact pads 2116 and bond pads 2114. That is, one or more

probe card assemblies may be used to contact only bond pads 2114 with one or more of spring contact elements 2118, and one or more additional probe card assemblies may be used to contact special contact pads 2116 with one or more spring contact elements 2120. In still other embodiments, multiple probe card assemblies may be used that have a mixture of spring contact elements 2118 and 2120.

For an alternative embodiment, bond pads 2116 and special contact pads 2116 may be of different heights. For example, as shown in Figure 22, bond pads 2114 may be taller than special contact pads 2116 (or vice versa). For this embodiment, probes 2118 and 2120 are extended to different depths (or have different heights). That is, probes 2120 may extend lower than probes 2118 to make contact with special contact pads 2116.

For an alternative embodiment, as shown in Figure 23, spring contact elements 2118 and 2120 may be attached to bond pads 2114 and special contact pads 2116 on die 2111. For this embodiment, space transformer 2110 may include pads 2120 to make contact with the spring contact elements 2118 and 2120. For yet another embodiment, some of the spring contact elements 2118 or 2120 may attached to space transformer 2110 and some may be attached to die 2111.

Figure 24 shows a side cross-sectional view of spring contact element 2400 that is one embodiment of the spring contact elements 2118 and 2120 of Figures 21-23. Spring contact element 2400 includes a base 2402, elongated resilient member 2404, an elongated contact tip structure 2406, and a pyramid-shaped contact feature 2408. Many other embodiments of spring contact elements may be used including those disclosed in commonly-owned, co-pending U.S. Application No. 08/526,246 filed on September 21, 1995, commonly-owned, co-pending U.S. Application No. 08/558,332 filed on November 15, 1995, commonly-owned, co-pending U.S. Application No.

08/789,147 filed on January 24, 1997, commonly-owned, co-pending U.S. Application No. 08/819,464 filed on March 17, 1997, commonly-owned, co-pending U.S. Application No. 09/189,761 filed on November 10, 1998, which are all incorporated by reference herein.

Structure 2406 can be any shape. Figure 25 shows one embodiment of structure 25 which includes a relatively wider end for contacting to member 2404, and a relatively narrower end for supporting pyramid-shaped contact feature 2408.

Figure 26 shows one embodiment of pyramid-shaped contact feature 2408. Other shapes may be used. Feature 2408 is advantageously be significantly smaller than typical tungsten probe tips of cantilevered probes and contact balls of C4 of flip-chip probe card technologies. The tip of pyramid-shaped contact feature 2408 may have a length 2414 and width 2416 dimensions of approximately 1 to 5 μm. For alternative embodiments, 2414 and 2416 may be submicron dimensions. The small size of contact 2408 may allow for special contact pads to be smaller that bond pads. As previously discussed, when the special contact pads are smaller that the bond pads, then the special contact pads can be added to an integrated circuit without increasing the die size. Additionally, smaller special contact pads can be placed between bond pads.

Figures 29A and 29B show side and perspective views, respectively, of another embodiment of a spring contact element disclosed in U.S. Application No. 09/189,761. Spring contact element 2900 is coupled to a substrate 2906 and includes an elongated resilient member 2904, tip structure 2908, and blade 2902. Blade 2902 is used to make electrical contact to bond pads or special contact pads. Blade 2902 may advantageously be used to provide a good electrical connection to contacted bond or special contact pads as blade 2902 may cut, slice, or otherwise penetrate the top surface of the pad.

Blade 2902 may be disposed substantially horizontally on tip structure 29A, or in any other orientation.

Figures 30A and 30B show perspective and side views, respectively, of another embodiment of using blades on tip structures of spring contact elements. Blade 3000 is a multi-height blade disposed on tip structure 3006. Blade 3000 has a primary blade 3002 toward the front edge of tip structure 3006, and a trailing blade 3004 toward the back of tip structure 3006.

Figure 31 shows a perspective view of another blade structure formed on a tip structure 3100. The blade of Figure 31 is formed having a substantially rectangular base 3102 and a substantially triangular shape 3104.

Figure 27 illustrates test system 2700 that is another embodiment for performing a wafer-level sort test of a die 2711. One embodiment of apparatus 2700 for testing more than one die at a time is described in commonly-owned, co-pending U.S. patent Application No. 08/784,862 filed on January 15, 1997, which is incorporated herein by reference.

Die 2711 includes bond pads 2714 and special contact pads 2716. Wafer 2712 includes die 2711 and may be disposed on a suitable support structure such as vacuum chuck 2726. Die 2711 may embody an integrated circuit such as integrated circuit 100 of Figures 1-6.

System 2700 includes a support chuck 2704 and a probe card assembly or test substrate. The probe card assembly includes an interconnection substrate (base plate) 2708, an active electronic component 2710, and spring contact elements 2718 and 2720. Component 2710 includes circuitry for applying test signals to, and monitoring the test output from, die 2711. For one embodiment, component 2710 may be an application-specific integrated circuit (ASIC).

Like host 1302 of Figure 13, host 2702 communicates test signals with the probe card assembly. For one embodiment, host 2702 communicates test

signals with component 2710 via interconnection substrate 2708. Power may be provided to component 2710 from power supply 2704.

System 2700 also includes guide pins 2722 disposed around the periphery of wafer 2712 and the probe card assembly to ensure accurate alignment when spring contact elements 2718 and 2720 are urged into contact with bond pads 2714 and special contact pads 2716, respectively. A compression stop (block ring) 2724, which may be suitably disposed on the face of wafer 2712, limits the amount of travel or distance that the tips of the spring contact elements 2718 and 2720 will deflect when urged against the pads of die 2711.

Spring contact elements 2718 are formed in a predetermined alignment to contact bond pads 2714. Probes 2718 may be arranged in a grid array to contact bond pads 2714 arranged on die 2711 in a corresponding grid array pattern. Spring contact elements 2720 may be aligned in the predetermined grid array, outside of the grid array pattern, or interspersed within the grid array pattern to align with corresponding special contact pads 2716. Alternatively, spring contact elements 2718 may be arranged in a peripheral pattern to contact bond pads 2714 arranged on die 2711 in a corresponding peripheral pattern. Spring contact elements 2720 may be arranged with the predetermined peripheral pattern, outside of the peripheral pattern, or within the peripheral pattern to align with corresponding special contact pads 2716. In yet another embodiment, spring contact elements 2718 may be arranged in a lead-on-center arrangement to align with lead-on-center bond pads on a die, and spring contact elements 2720 may be arranged within or outside of the lead-on-center arrangement to align with corresponding special contact pads.

While Figure 27 shows that a single probe card assembly may be used to communicate with special contact pads 2716 and bond pads 2714, in alternative embodiments, separate probe card assemblies may be used for

probing special contact pads 2716 and bond pads 2714. That is, one or more probe card assemblies may be used to contact only bond pads 2714 with one or more of spring contact elements 2718, and one or more additional probe card assemblies may be used to contact special contact pads 2716 with one or more spring contact elements 2720. In still other embodiments, multiple probe card assemblies may be used that have a mixture of spring contact elements 2718 and 2720.

For an alternative embodiment, bond pads 2716 and special contact pads 2716 may be of different heights. For example, bond pads 2714 may be taller than special contact pads 2716 (or vice versa). For this embodiment, probes 2718 and 2720 are extended to different depths (or have different heights). That is, probes 2720 may extend lower than probes 2718 to make contact with special contact pads 2716.

For an alternative embodiment, spring contact elements 2718 and 2720 may be attached to bond pads 2714 and special contact pads 2716 on die 2711. For this embodiment, component 2710 may include pads to make contact with the spring contact elements. For yet another embodiment, some of the spring contact elements 2718 or 2720 may be attached to component 2710 and some may be attached to die 2711.

As previously described above, special contact pads can be disposed on a die or on packages such as Land Grid Array (LGA) packages. When special contact pads are disposed on packages or on devices arranged in a C4 or flip-chip configuration, they can provide a means for supplying test signals or programming signals to the special contact pad of the die. This may be advantageous to allow, for example, field programming of packaged programmable logic device or nonvolatile devices without having to provide dedicated bonded out pins for the programming function. Additionally, embedded nonvolatile memory arrays that store program code, application

software, or BIOS may be updated in the field. Special contact pads disposed on a package may also provide an advantageous means for testing a faulty device and programming redundant circuits to replace a faulty circuit as described above with respect to Figures 8-10.

Figure 28 illustrates one embodiment of solder-down (surface mount) LGA socket 2800 for mounting to a printed circuit board (PCB) substrate 2810 and for making pressure contacts to bond pads 2812 and special contact pads 2814 of LGA package 2804. As used herein, the term "socket" refers to an electronic component having interconnection elements, suitable for making electrical connection to terminals or connection points of another electronic component. The socket shown in Figure 28 is intended to permit a semiconductor package to be removably connected to a circuit board. Other embodiments of socket 2800 are disclosed in commonly-owned U.S. Patent No. 5,772,451 which is incorporated herein by reference.

PCB 2810 has a plurality of terminals or pads 2818, and package 2804 have a plurality of bond pads 2812 and special contact pads 2814. Socket 2800 provides a means for electrically interconnecting terminals 2818 with pads 2812 and 2814. Circuitry provided on PCB 2810, or in communication therewith, may provide signals to or monitor signals from pads 2812 and 2814 through socket 2800. For example, programmable circuitry within package 2804 may be programmed or monitored through spring contact elements 2816, special contact pads 2814 and/or pads 2812.

Socket 2800 includes a support substrate 2808 formed, for example, from a conventional PCB material. Support substrate 2808 includes spring contact elements 2816 formed on a top surface thereof, and pads 2822 formed on a bottom surface thereof. Spring contact elements 2816 are for contacting pads 2812 and 2814 of package 2804 when package 2804 is urged downward by a forced applied to the topside of package 2804 by retaining means 2802. Other

contact elements besides spring contact elements may also be used. Support substrate 2808 also includes electrical conduits 2824 that provide an electrical interconnection between spring contact elements 2816 and pads 2822. For an alternative embodiment, spring contact elements 2816 may be connected directly to terminals 2818.

Contact balls (such as conventional solder balls) are disposed on the bottom surface of pads 2822. The contact balls 2822 serve as contact structures disposed on the bottom surface of the support substrate 2808 to contact corresponding pads or terminals 2818 on PCB 2810. Other electrical contact structures may also be used.

Socket 2800 also includes a frame 2806 that is attached to PCB 2802. Frame 2806 includes landings 2826 to support package 2804. Socket 2800 also includes retaining means 2802 that is disposed over frame 2826 and package 2804. Retaining means 2802 retains package 2804 on landings 2826 such that spring contact elements 2816 remain in electrical contact with pads 2812 and 2814. Any suitable mechanical means may be used for retaining means 2802 including, for example, a spring clip.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

circuitry;

a bond pad coupled to the circuitry and for interfacing the circuitry with an external circuit; and

a special contact pad coupled to the circuitry, the special contact pad for use only when testing the circuitry.

2. The integrated circuit of claim 1, wherein the special contact pad is smaller than the bond pad.

3. The integrated circuit of claim 1, wherein the special contact pad has a maximum dimension of approximately 10 microns.

4. The integrated circuit of claim 1, wherein the special contact pad is structured to receive a spring contact element.

5. The integrated circuit of claim 1, wherein the special contact pad is for communicating test data to the circuitry.

6. The integrated circuit of claim 1, wherein the special contact pad is for communicating data from the circuitry.

7. The integrated circuit of claim 1, wherein the special contact pad is for contacting a circuit node internal to the circuitry.

8. An integrated circuit comprising:

a plurality of circuits;

a plurality of bond pads each coupled to at least one of the plurality of circuits, the plurality of bond pads for interfacing the plurality of circuits with circuits external to the integrated circuit; and

a plurality of special contact pads each coupled to at least one of the plurality of circuits and providing an electrical contact for communicating with the plurality of circuits.

9. The integrated circuit of claim 8, wherein the bond pads are arranged in a first predetermined alignment and the special contact pads are arranged in a second predetermined alignment.

10. The integrated circuit of claim 8, wherein the bond pads are disposed along the periphery of the integrated circuit, and at least one of the special contact pads is not disposed on the periphery of the integrated circuit.

11. The integrated circuit of claim 8, wherein the bond pads are aligned in a grid pattern on the integrated circuit, and at least one of the special contact pads is not aligned in the grid pattern.

12. The integrated circuit of claim 8, wherein the bond pads are aligned in a lead-on-center configuration, and at least one of the special contact pads is not aligned in the lead-on-center configuration.

13. The integrated circuit of claim 8, wherein the special contact pads are smaller than the bond pads.

14. The integrated circuit of claim 8, further comprising a spring contact element attached to one of the special contact pads.

15. The integrated circuit of claim 8, wherein at least one of the special contact pad is electrically disposed between two of the plurality of circuits to monitor signals transmitted between circuits.

16. The integrated circuit of claim 8, wherein one of the special contact pads communicates test data to one of the circuits, and another one of the special contact pads communicates an output of the circuit.

17. The integrated circuit of claim 8, wherein one of the special contact pads communicates test data to the one of the circuits, and one of the bond pads communicates an output of the circuit.

18. The integrated circuit of claim 8, wherein one of the bond pads communicates test data to one of the circuits, and one of the special contact pads communicates an output of the circuit.

19. The integrated circuit of claim 8, wherein in a first mode of operation one of the special contact pads communicates data to one of the circuits, and in a second mode of operation the special contact pads communicates data from the circuit.

20. The integrated circuit of claim 8, wherein one of the plurality of circuits is an embedded memory array, and the special contact pads communicates address and test data to the embedded memory array.

21. The integrated circuit of claim 8, wherein one of the plurality of circuits includes programmable circuitry, and the special contact pads are for communicating signals for programming the programmable circuitry.

22. The integrated circuit of claim 8, wherein the bond pads are structured to be connected to external circuitry by bonding wires, and the special contact

pads are not structured to be connected to external circuitry by bonding wires.

23. The integrated circuit of claim 8, wherein the bond pads are structured to be connected to external circuitry by solder bumps, and the special contact pads are not structured to be connected to external circuitry by solder bumps.

24. The integrated circuit of claim 8, wherein the bond pads are structured to be in electrical contact with a package for housing the integrated circuit, and the special contact pads are not structured to be in electrical contact with the package.

25. The integrated circuit of claim 8, wherein the plurality of circuits includes a first circuit and a second circuit having a redundant function of the first circuit, and wherein the special contact pads are disposed about the first and second circuits to communicate with the first and second circuits.

26. The integrated circuit of claim 25, further comprising means for communicating with the special contact pads and for disabling the first circuit if it is defective and for enabling the second circuit.

27. The integrated circuit of claim 25, further comprising means for communicating with the special contact pads and for disabling the second circuit.

28. The integrated circuit of claim 8, further comprising electrostatic discharge protection circuitry for the bond pads and not for the special contact pads.

29. An integrated circuit comprising:

a plurality of bond pads;

an internal circuit not directly monitorable by the bond pads; and

at least one special contact pad for directly accessing the internal circuit.

30. The integrated circuit of claim 29, wherein the internal circuit comprises an embedded memory array, and the at least one special contact pad communicates address and memory data with the embedded memory array.

31. The integrated circuit of claim 29, wherein the internal circuit comprises programmable circuitry, and the at least one special contact pad communicates programming signals to the programmable circuitry.

32. The integrated circuit of claim 29, wherein the bond pads are arranged in a first predetermined alignment and the at least one special contact pad is in a second predetermined alignment.

33. The integrated circuit of claim 29, wherein the at least one special contact pad is smaller than the bond pads.

34. The integrated circuit of claim 29, further comprising a spring contact element attached to the at least one special contact pad.

35 A package for housing an integrated circuit, comprising:

a plurality of terminals for testing the overall operation of the integrated circuit; and

a special contact pad for directly accessing an internal circuit of the integrated circuit.

36. The package of claim 35, wherein the special contact pad is for communicating test signals for the integrated circuit.

37. The package of claim 35, wherein the special contact pad is for communicating test signals from the integrated circuit.

38. The package of claim 35, wherein the contact pads are aligned in a grid pattern on the integrated circuit, and the special contact pads is not aligned in the grid pattern.

39. The package of claim 35, wherein the package comprises a ball-grid-array (BGA) package and the contact pads include contact balls.

40. The package of claim 35, wherein the special contact pad is smaller than the contact pad.

41. The package of claim 35, wherein the special contact pad has a maximum dimension of approximately 10 microns.

42. A method of testing circuitry in an integrated circuit having bond pads and a special contact pad, the method comprising:

providing test signals to the circuitry; and

monitoring an output of the circuitry through the special contact pad.

43. A method of testing circuitry in an integrated circuit having bond pads and a special contact pad, the method comprising:

providing test signals to the circuitry through the special contact pad; and

monitoring an output of the circuitry through the bond pad.

44. A method of testing an integrated circuit having bond pads and a special contact pad, the method comprising:

providing test signals to a first circuit through at least one of the bond pads;

monitoring an output of the first circuit through the special contact pad;

providing the output of the first circuit to a second circuit; and

providing an output of the second circuit to at least another one of the bond pads.

45. A method of testing an integrated circuit on a wafer, comprising:

electrically contacting a first test substrate to special contact pads disposed on the integrated circuit; and

electrically contacting a second test substrate to bond pads disposed on the integrated circuit.

46. A probe card comprising:

a first probe element for contacting bond pads of an integrated circuit; and

a second probe element for contacting a special contact pad of the integrated circuit

47. The probe card of claim 46, wherein the first and second probe elements comprise cantilevered probes.

48. The probe card of claim 46, wherein the first and second probe elements comprise contact balls.

49. The probe card of claim 46, further comprising a plurality of the first probe elements arranged in a first predetermined alignment, and wherein the second probe element is arranged in a second predetermined alignment.

50. The probe card of claim 49, wherein the predetermined alignment is a grid pattern.

51. The probe card of claim 49, wherein the predetermined alignment is a rectangular pattern.

52. The probe card of claim 49, wherein the first and second probe elements have different lengths.

53. The probe card of claim 49, wherein the first and second probe elements are spring contact elements.

54. The probe card of claim 53, wherein the spring contact elements include pyramid-shaped tip contact structures.

55. The probe card of claim 49, wherein the first and second probe elements are COBRA-style probes.

56. An apparatus for communicating signals with an internal circuit node and input/output (I/O) node of a semiconductor device, comprising:

a first contact element for communicating signals with the internal circuit node; and

a second contact element for communicating signals with the I/O node.

57. The apparatus of claim 56, wherein the first contact element comprises a resilient contact element.

58. The apparatus of claim 57, wherein the second contact element comprises a resilient contact element.

59. The apparatus of claim 56, wherein the first and second contact elements have different lengths.

60. A method of communicating a signal to an internal circuit node of a semiconductor device, comprising:

contacting a special contact pad that is electrically coupled to the internal circuit node; and

transferring electrical energy through the special contact pad to the internal circuit node.

61. A socket for releasably connecting a first electronic component to a second electronic component, comprising:

a first plurality of resilient contact structures extending upward from a top surface of a support substrate, the first plurality of resilient contact structures for communicating signals with a first plurality of contact points of the first electronic component;

a second plurality of resilient contact structures extending upward from the top surface of the support substrate, the second plurality of resilient contact structures for communicating signals with a second plurality of contact points of the second first electronic component; and

a plurality of contact structures disposed on a bottom surface of the support substrate, selected ones of the contact structures are connected through the support substrate to selected ones of the resilient contact structures.

62. The socket of claim 61, wherein the second electronic component is a circuit board.

63. The socket of claim 61, further comprising means for receiving the first electronic component.

64. The socket of claim 61, further comprising means for urging the first electronic component down onto the first and second resilient contact elements.

ABSTRACT OF THE DISCLOSURE

One embodiment of the present invention concerns an integrated circuit that includes bond pads and special contact pads or points. The bond pads are for interfacing the integrated circuit as a whole with an external circuit, and are to be bonded to a package or circuit board. The bond pads are disposed on the die in a predetermined alignment such as a peripheral, grid, or lead-on-center alignment. The special contact pads are used to provide external test patterns to internal circuits and/or to externally monitor results from testing the internal circuits. The special contact pads may be advantageously located on the integrated circuit with a high degree of positional freedom. For one embodiment, the special contact pads may be disposed on the die at a location that is not in the same alignment as the bond pads. The special contact pads may be smaller than the bond pads so as not to increase the die size due to the special contact pads. The special contact points may also be used to externally program internal circuits (e.g., nonvolatile circuits) at the die or package level. The special contact points may also be used to select redundant circuits for faulty circuits.

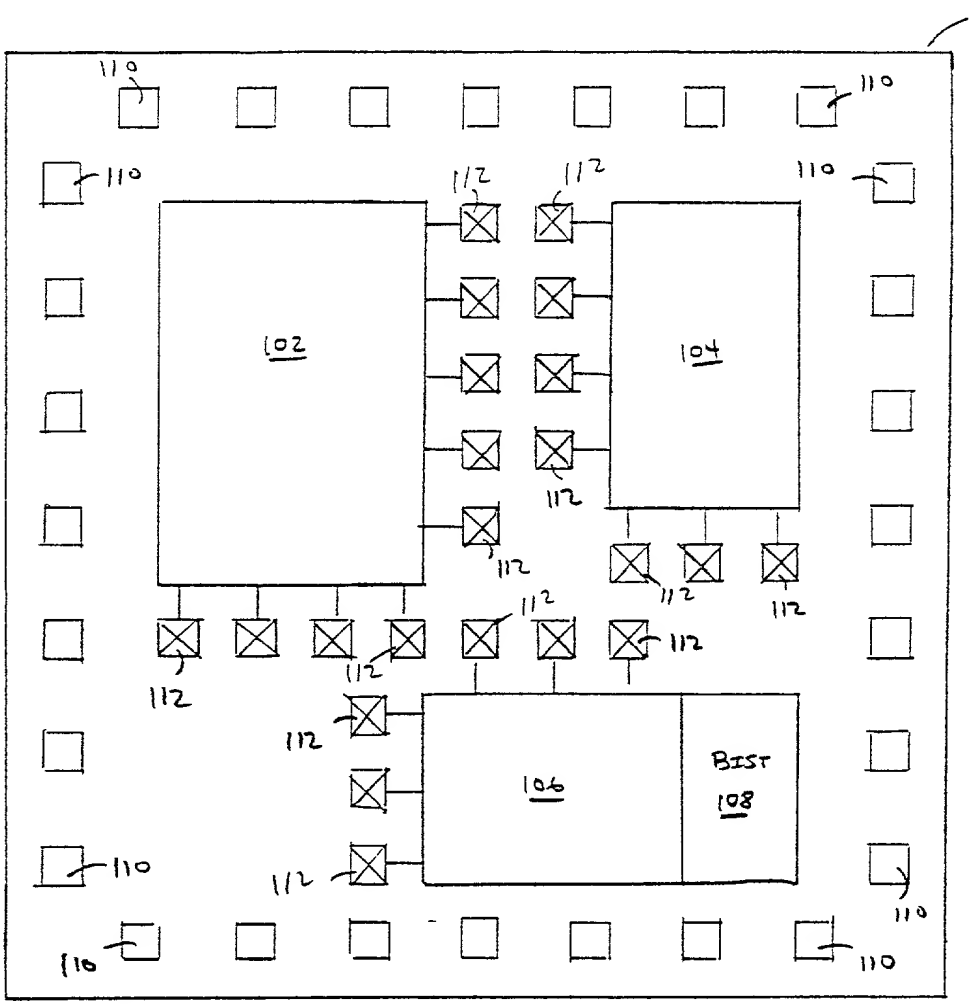


FIG. 1

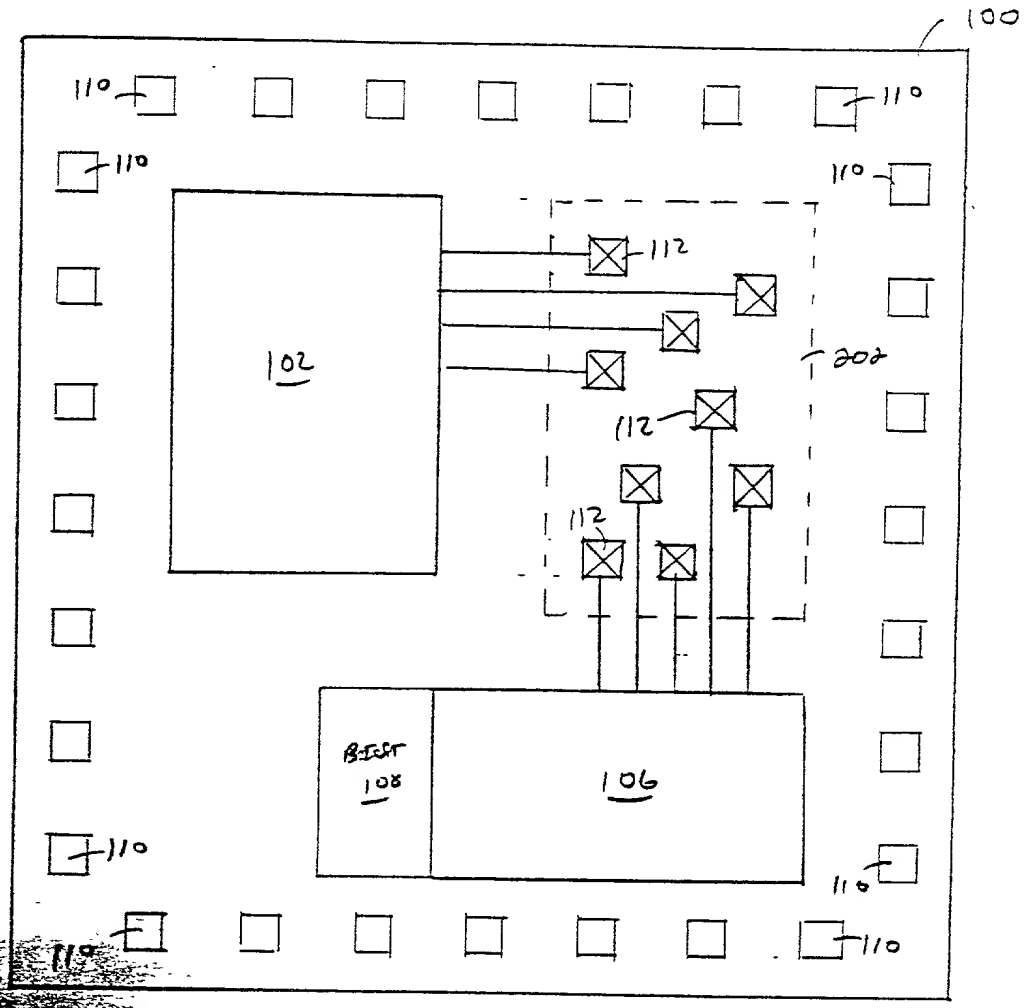


FIG. 2

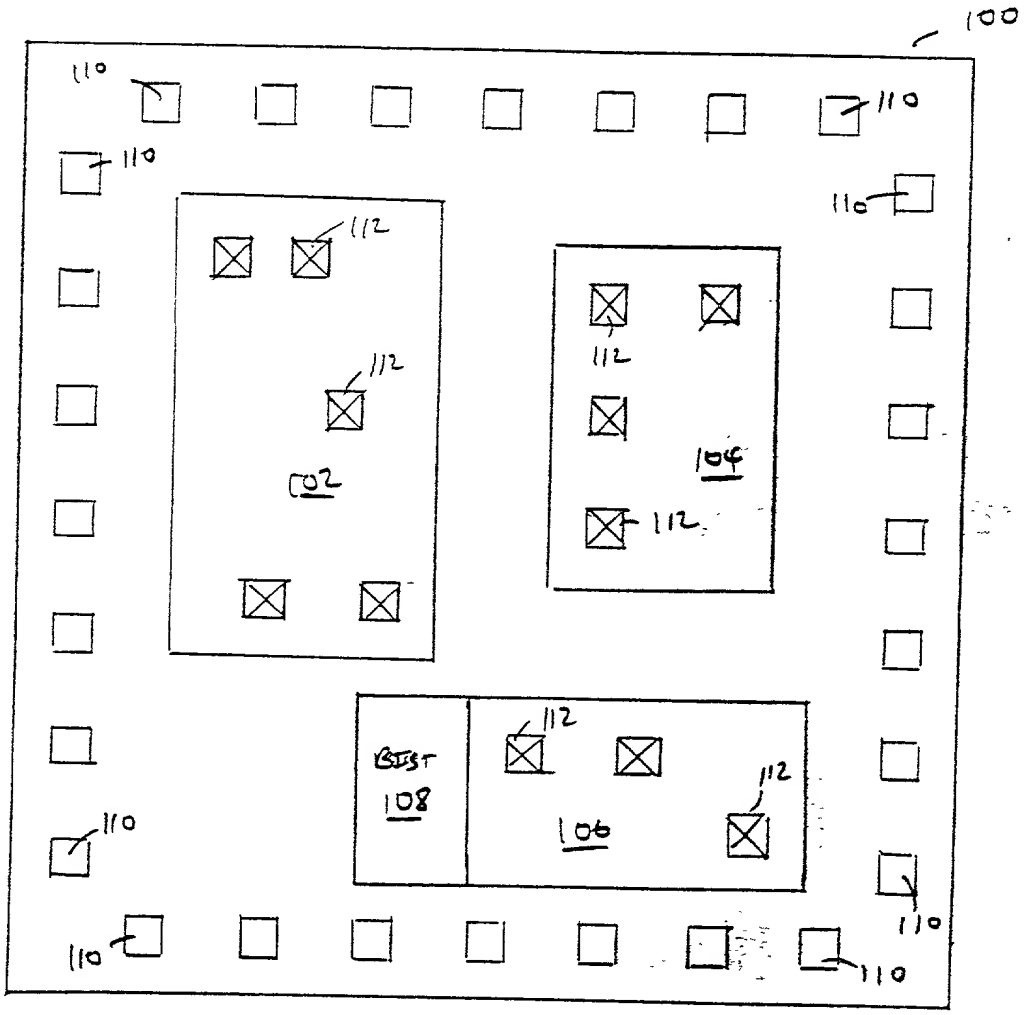


FIG. 3A

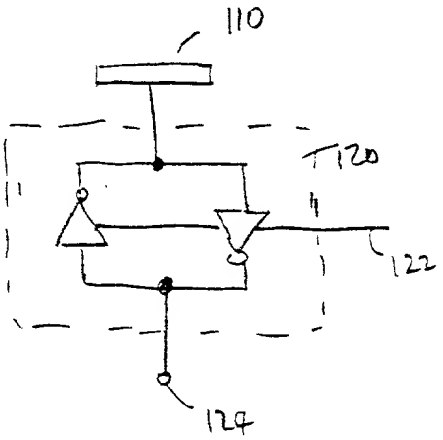


FIG. 3B

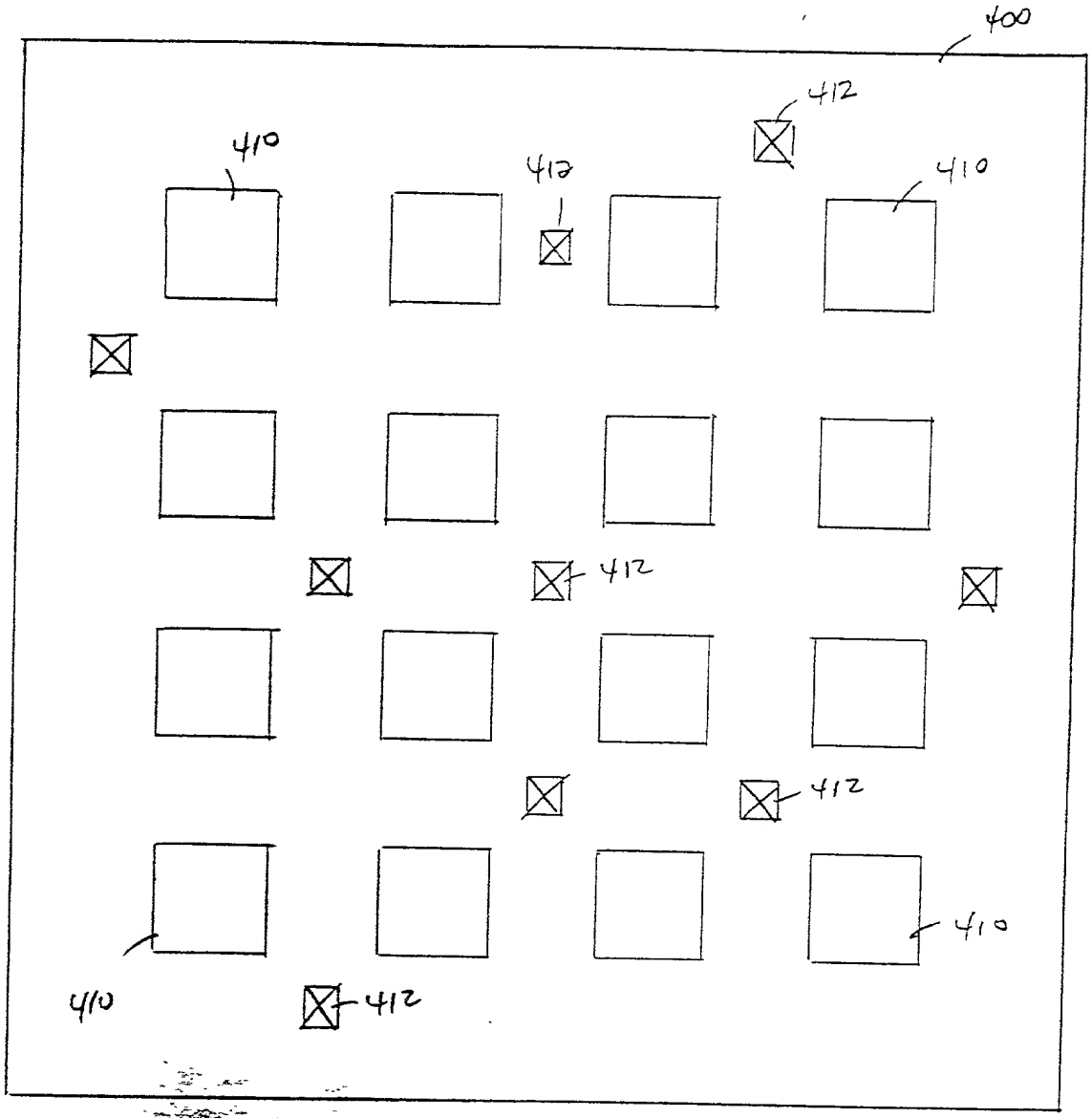


FIG. 4

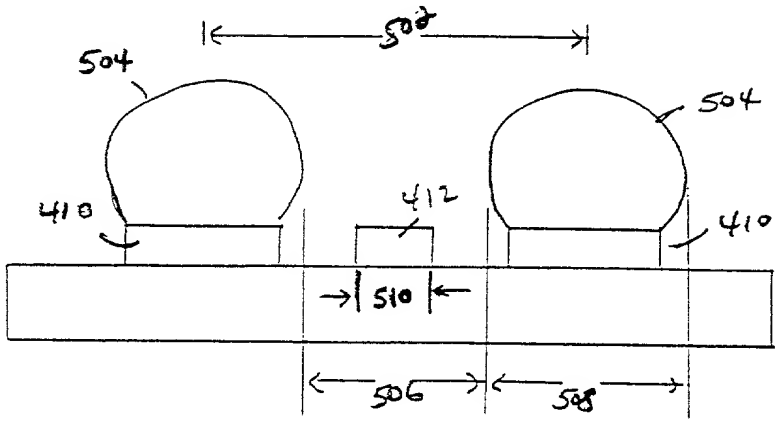


FIG. 5

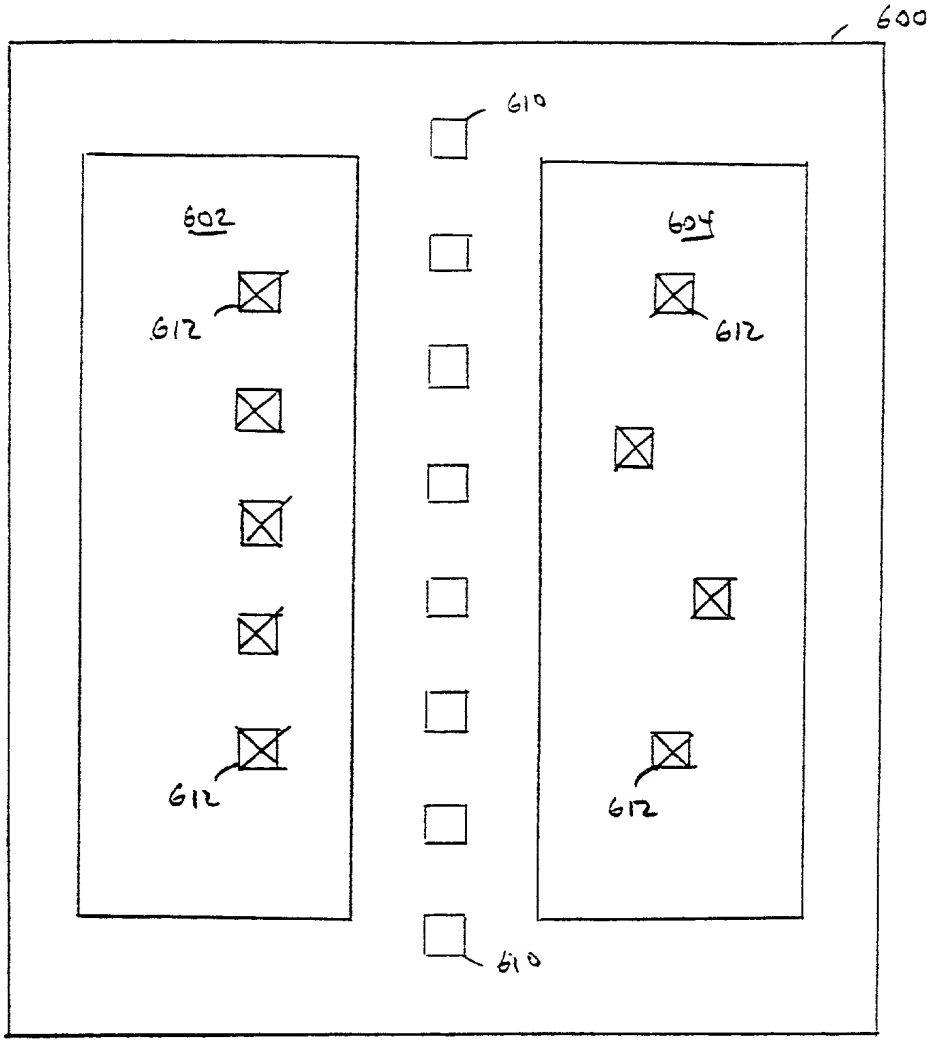


FIG. 6

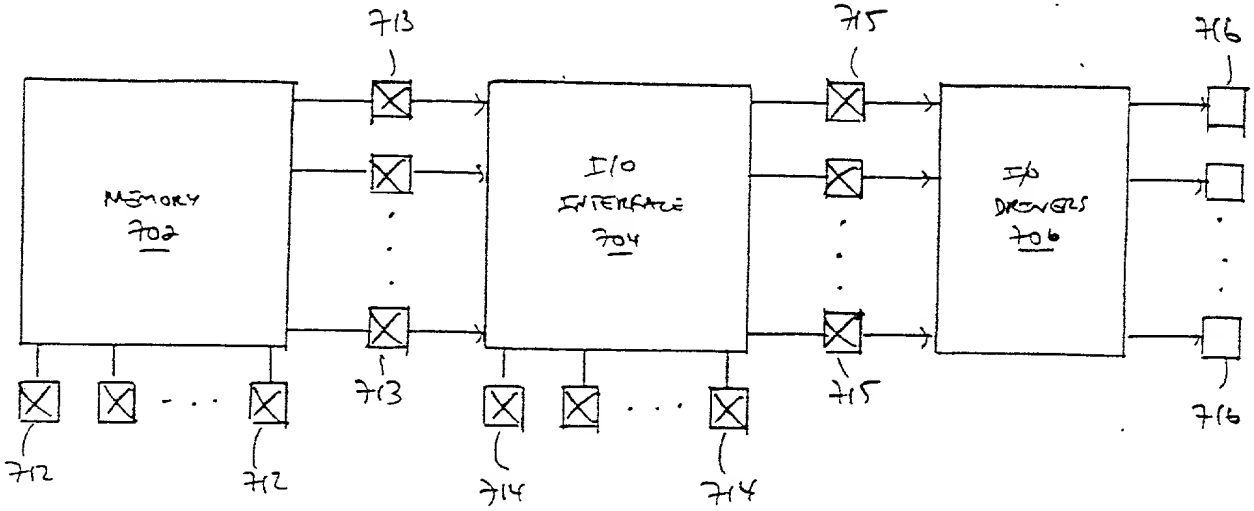


FIG. 7

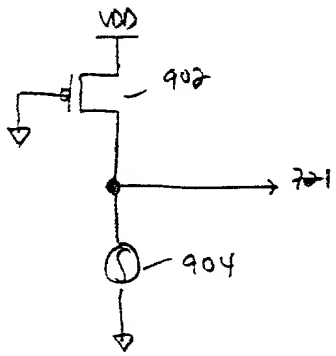


FIG. 9

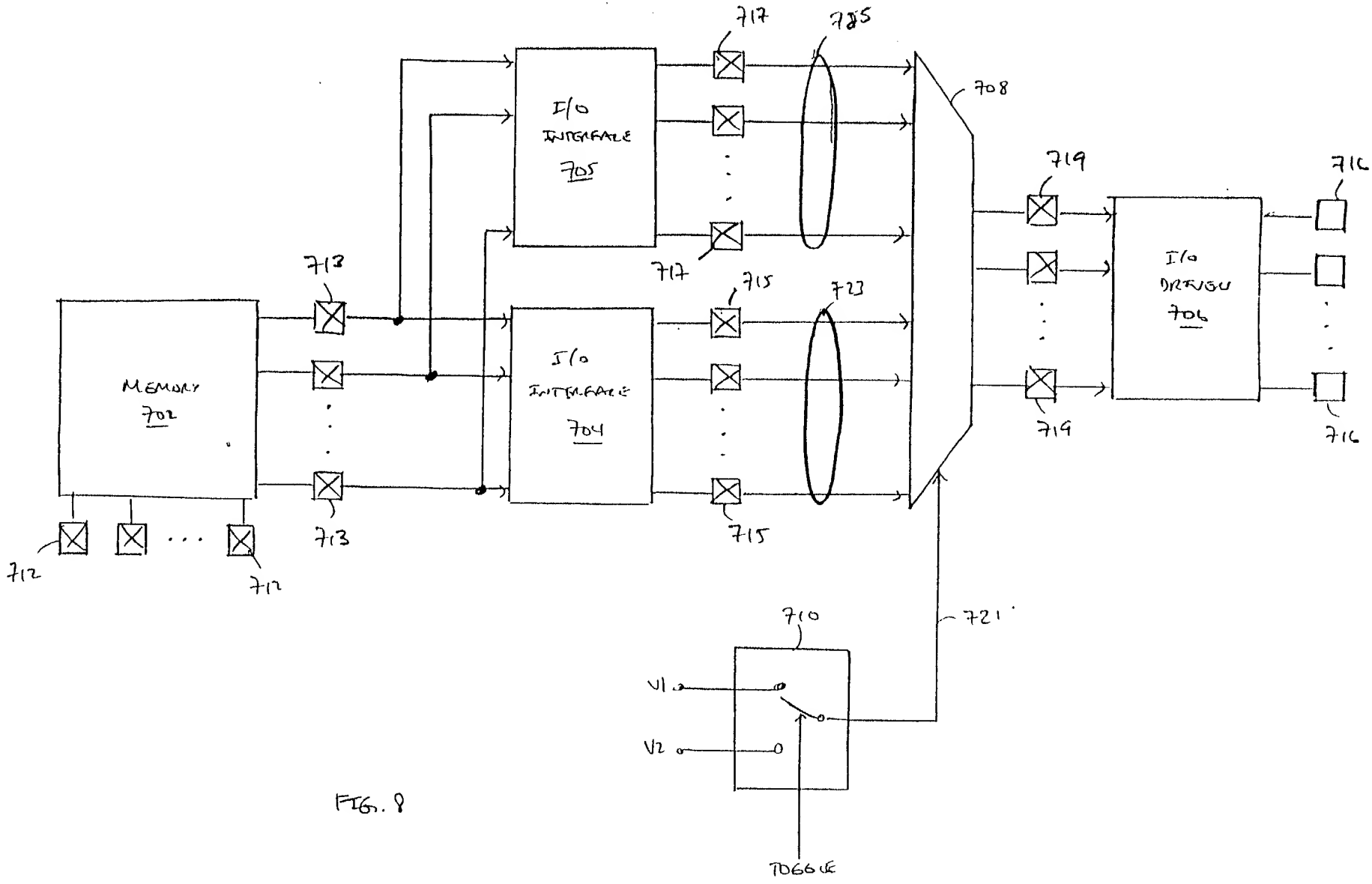


FIG. 8

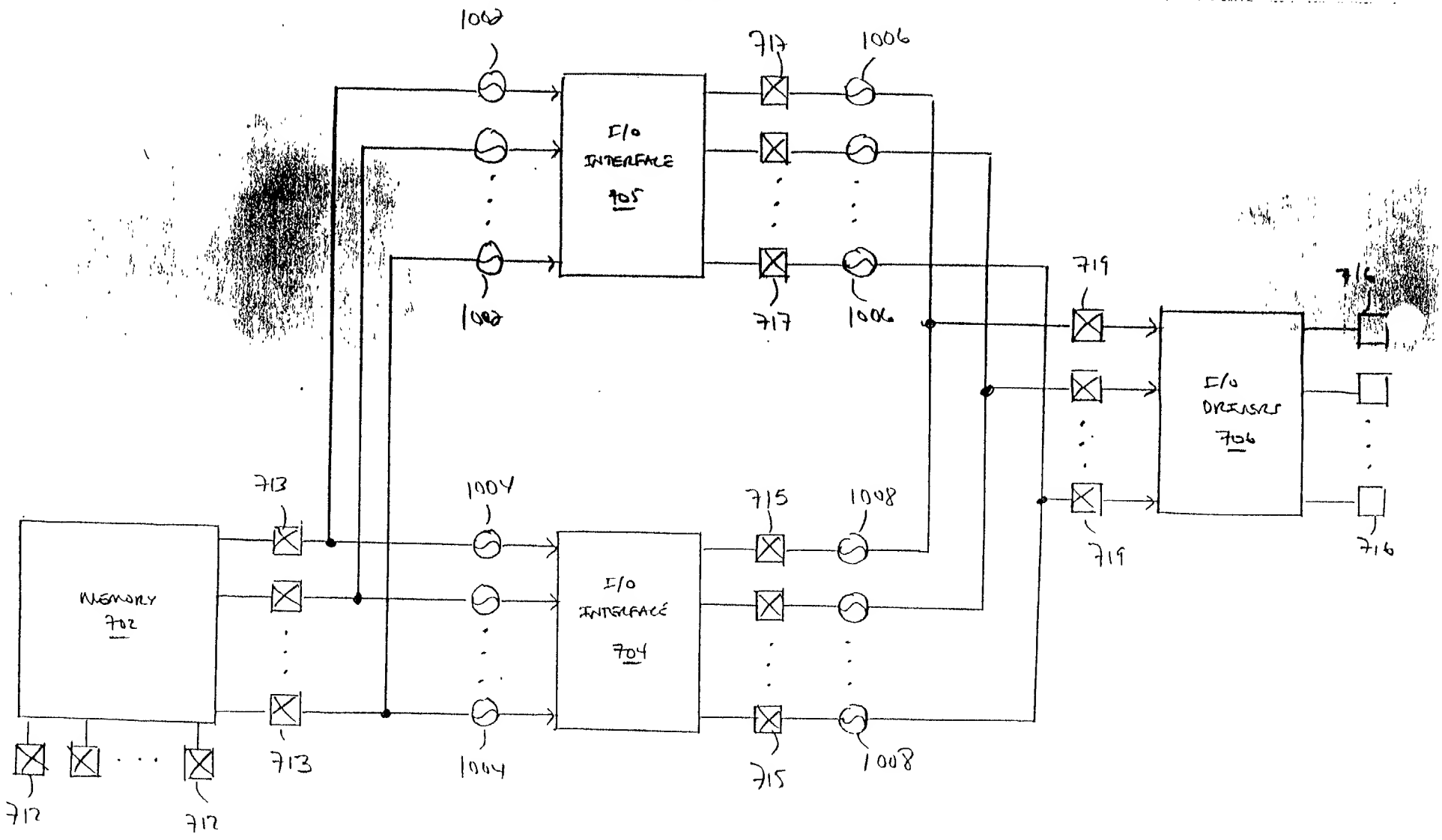


FIG. 10

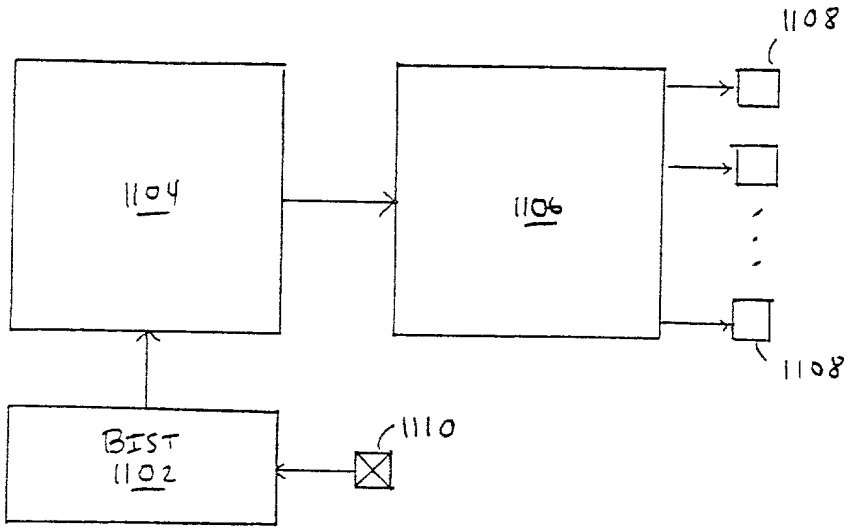

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FIG. 11

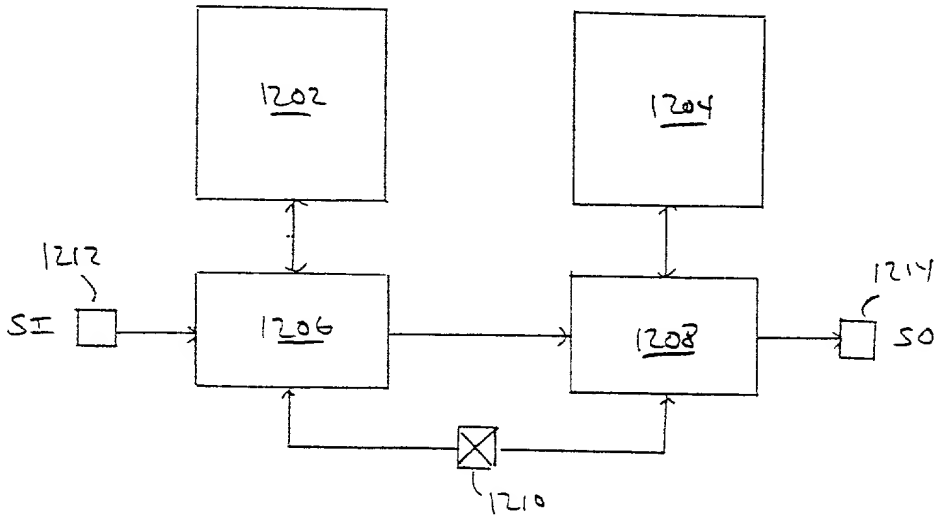
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FIG 12

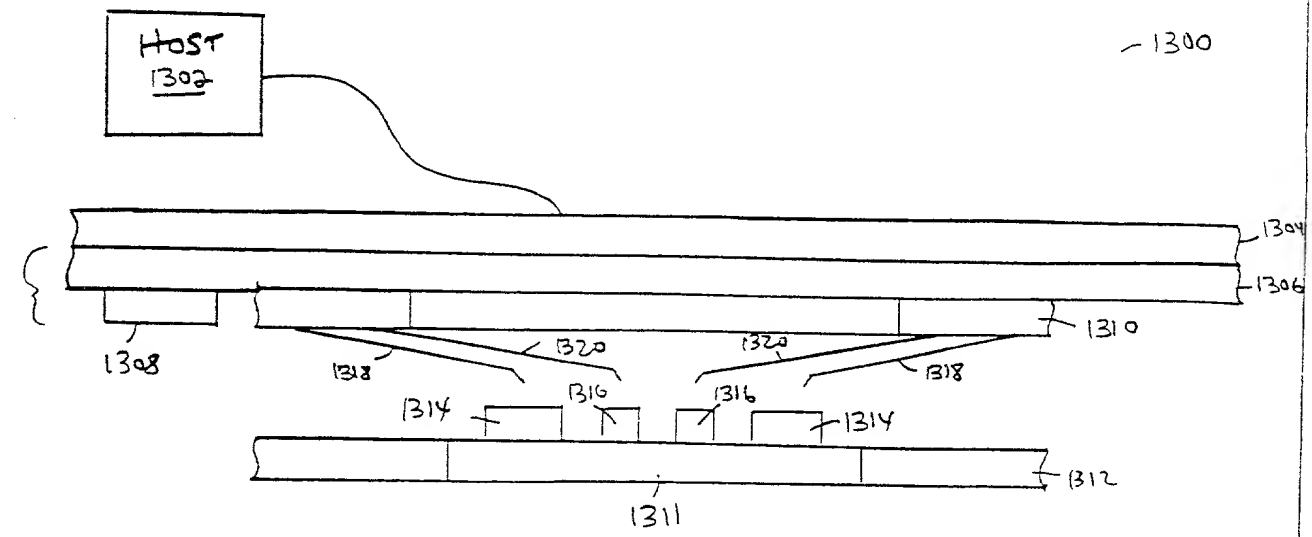
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FIG. 13

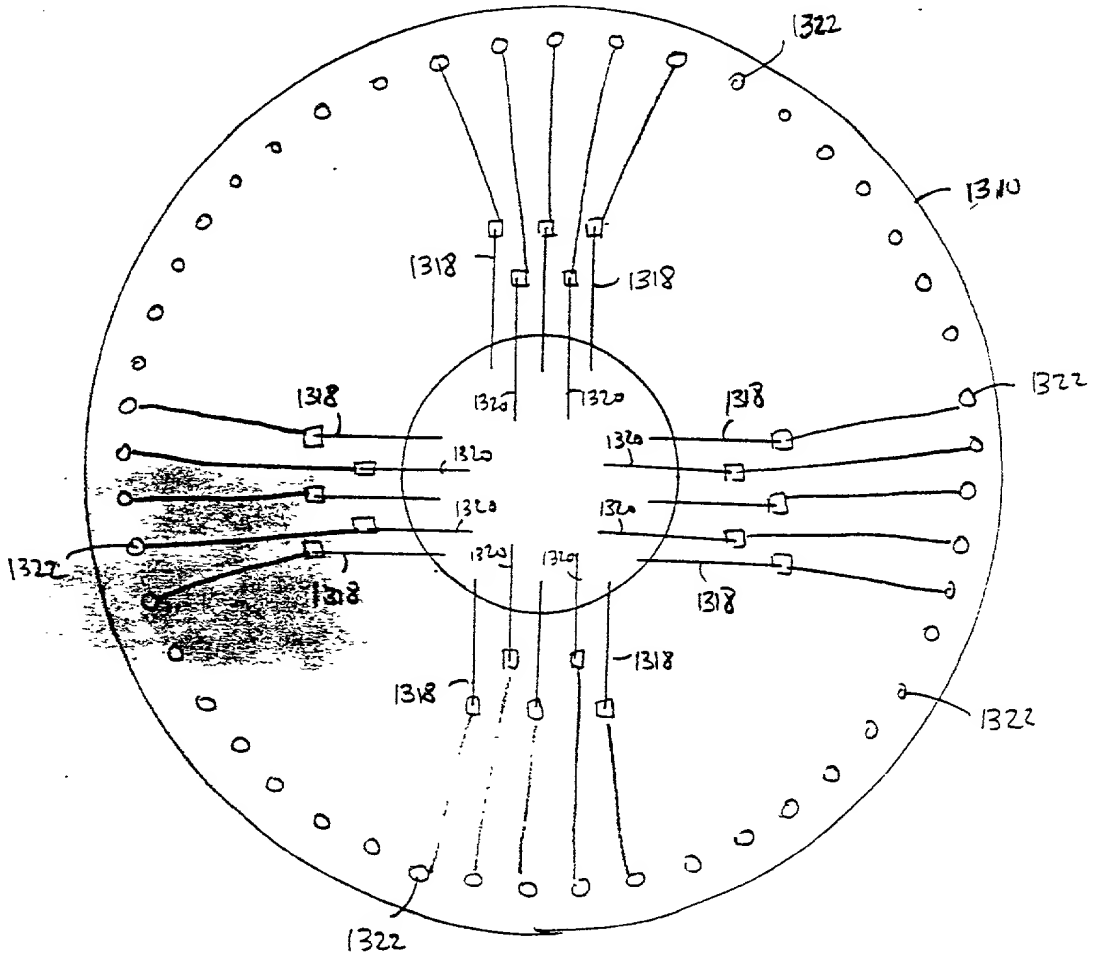
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FIG. 14

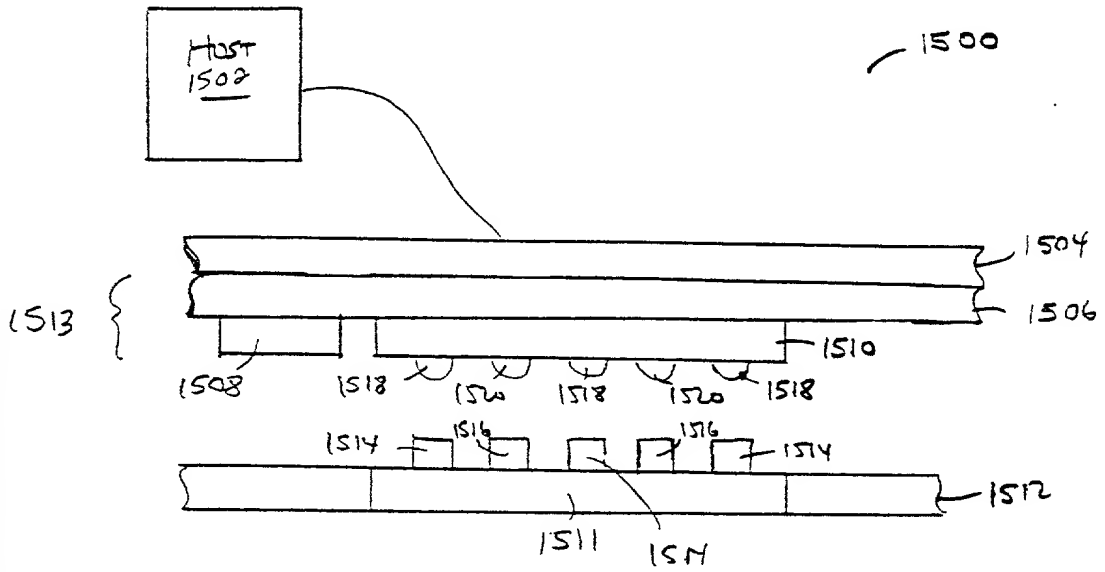

FIG. 15

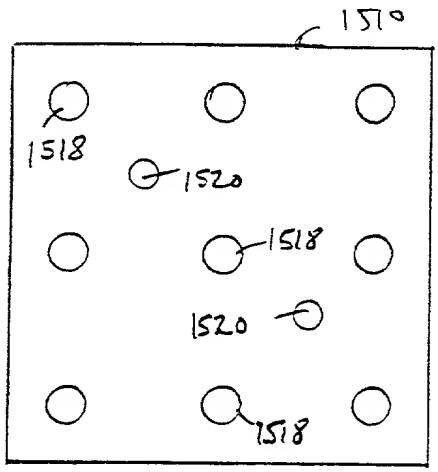

FIG. 16

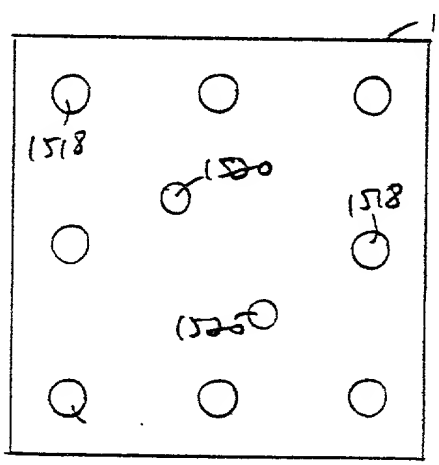

FIG. 17

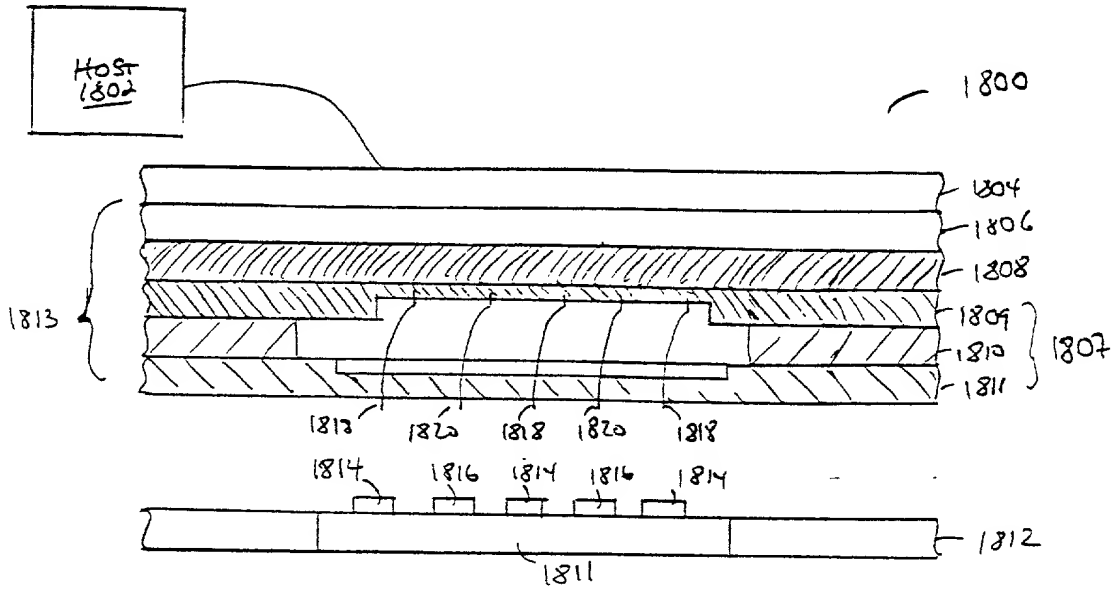

FIG. 18

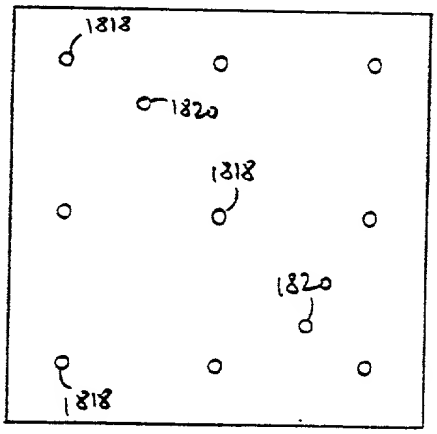

FIG 19

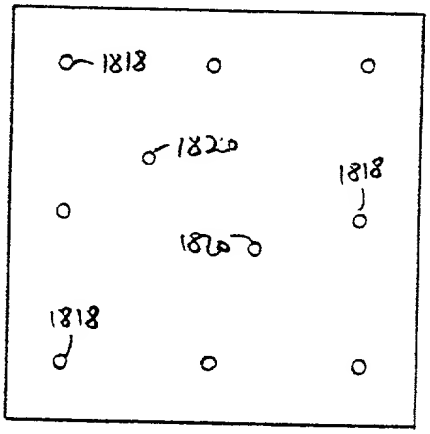

FIG 20

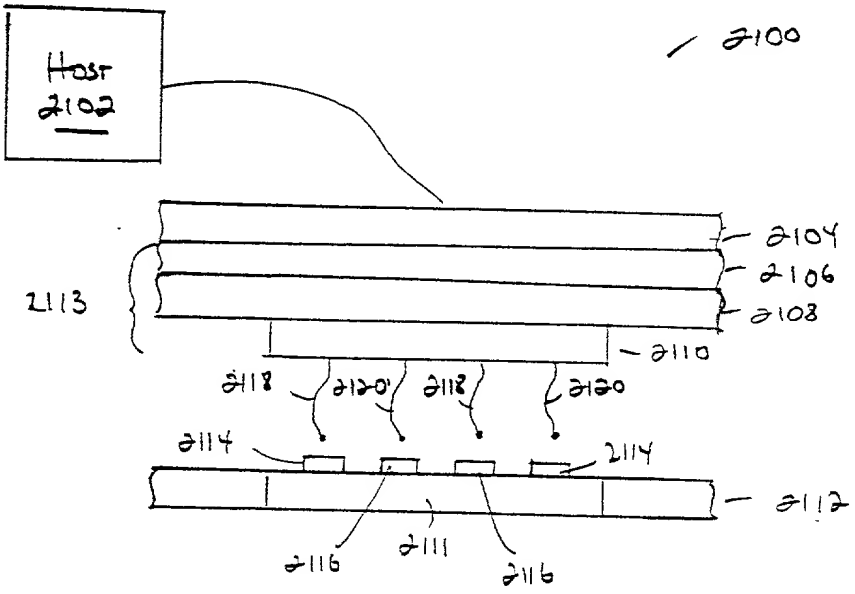

FIG. 21

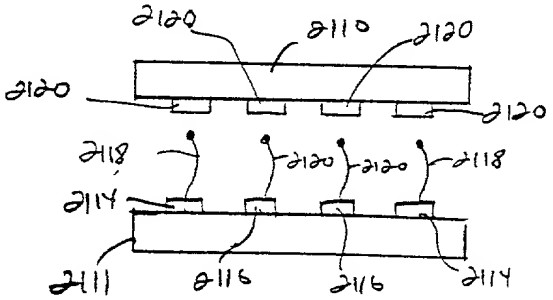

FIG. 23

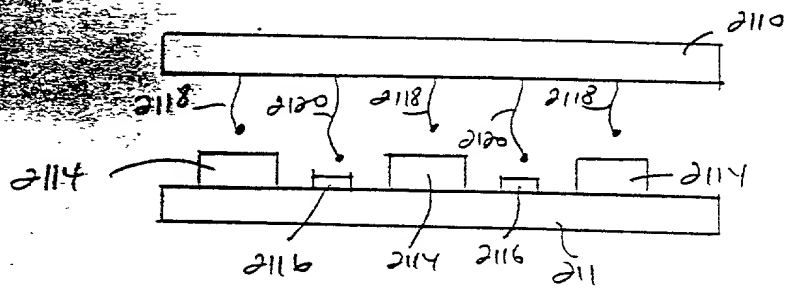

FIG 22

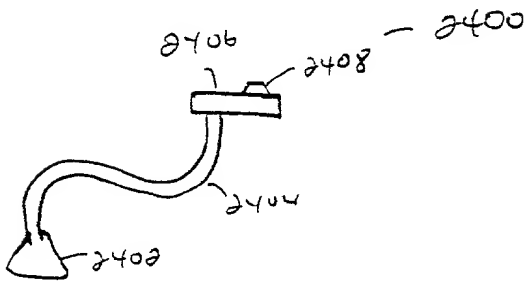

FIG. 24

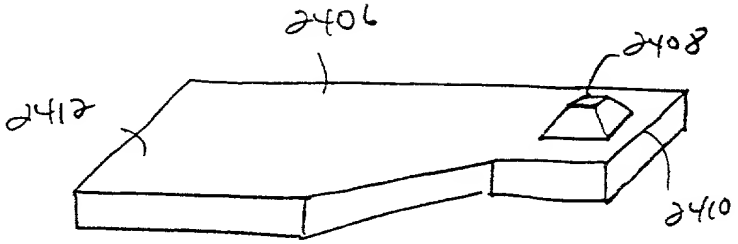

FIG. 25

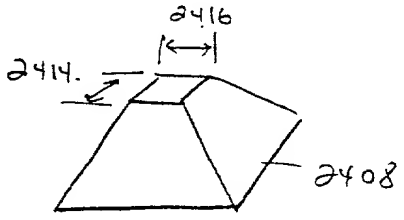

FIG. 26

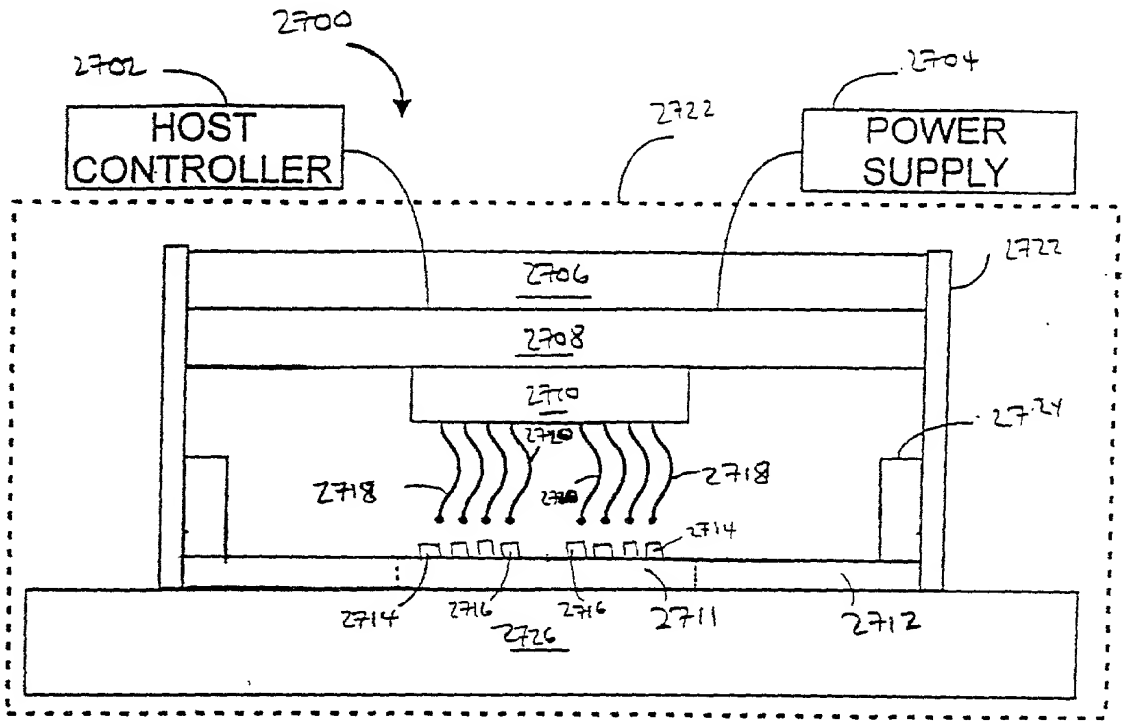
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FIG. 27

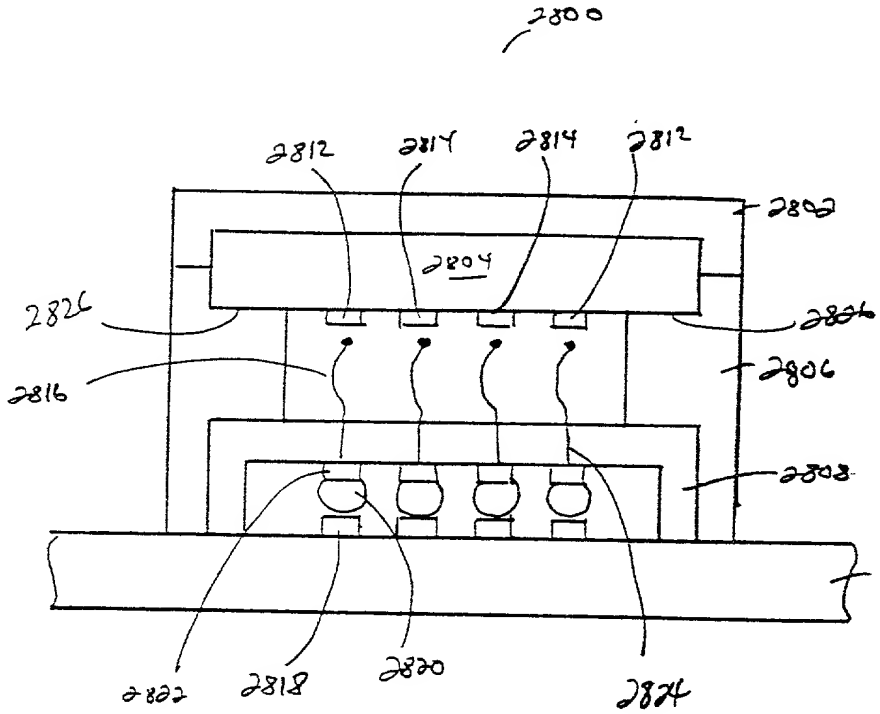
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FIG. 28

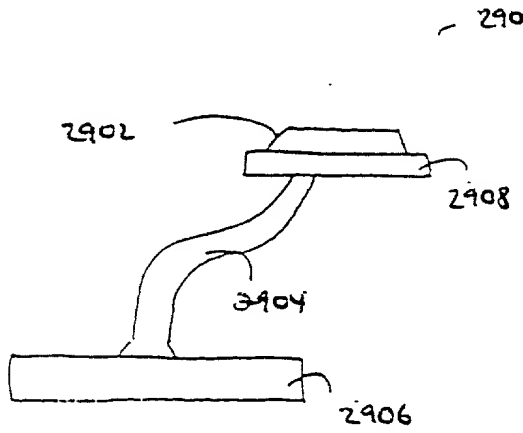

FIG. 29A

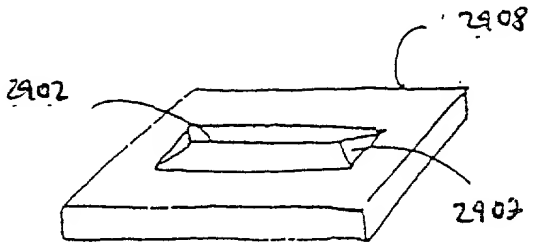

FIG. 29B

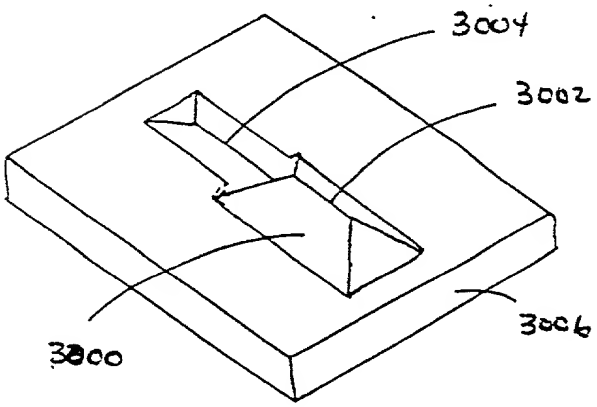

FIG. 30A

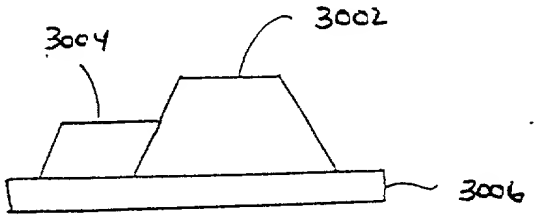

FIG. 30B

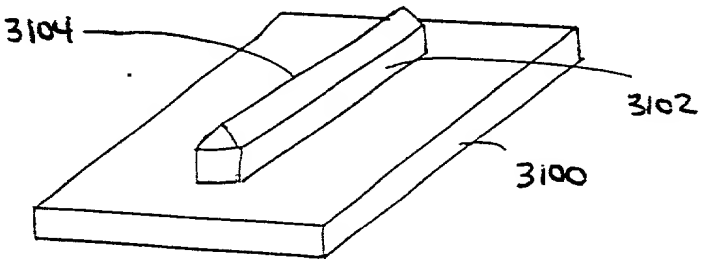

FIG. 31

This copy of the declaration is intended for the attached application (attorney docket no. P60D1-US) submitted herewith.
Express mail no. EE412508842US.

Attorney's Docket No.: 003401.P060 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SPECIAL CONTACT POINTS FOR ACCESSING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT

the specification of which

___ is attached hereto.
_X_ was filed on December 31, 1998 as
United States Application Number 09/224,169
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith. I also hereby appoint David Larwood, Reg. No. 33,191, my attorney; of FORMFACTOR, INC., located at 5666 La Ribera Street, Livermore, California, 94550, telephone (510)294-4300, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Roland B. Cortes, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Roland B. Cortes, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Benjamin N. Eldridge

Inventor's Signature _____ Date 19 MARCH 1999

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Full Name of Second/Joint Inventor Igor Y. Khandros

Inventor's Signature _____ Date 19 MARCH 1999

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Orinda, CA 94563

Full Name of Third/Joint Inventor David V. Pedersen

Inventor's Signature _____ Date 19 March 1999

Residence Scotts Valley, California (City, State) Citizenship USA (Country)

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Scotts Valley, CA 95066

Full Name of Fourth/Joint Inventor Ralph G. Whitten

Inventor's Signature _____ Date 3-19-99

Residence San Jose, California (City, State) Citizenship USA (Country)

Post Office Address 5220 Sierra Road
San Jose, CA 95132

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

PATENT
Docket No.: P60-US

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL" 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail on December 29, 2000 in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

N. Kenneth Burrast

This copy of the power of attorney is intended for the attached application (attorney docket no. P60D1-US) submitted herewith.
Express mail no. EE412508842US.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Eldridge et al.

Application No.: 09/224,169

Filing Date: December 31, 1998

For: SPECIAL CONTACT POINTS FOR ACCESSING INTERNAL CIRCUITRY OF AN INTEGRATED CIRCUIT

Examiner: Jimmy Nguyen

Group Art Unit: 2858

JC918 U.S. PTO 09/753309 12/29/00

REVOCATION AND POWER OF ATTORNEY BY ASSIGNEE TO EXCLUSION OF INVENTOR UNDER 3.71 AND CHANGE OF CORRESPONDENCE ADDRESS

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The undersigned Assignee of the entire interest in the above-identified application for letters patent hereby revokes all previous powers of attorney and appoints: Stuart L. Merkadeau, Reg. No. 33,262, and N. Kenneth Burraston, Reg. No. 39,923, to prosecute this application and transact all business in the U.S. Patent and Trademark Office connected therewith; said appointment to be to the exclusion of the inventors and the inventors' attorneys in accordance with the provisions of 37 C.F.R. § 3.71.

The following evidentiary documents establish a chain of title from the original owner to the Assignee:

☐ A copy of an Assignment attached hereto, which Assignment has been (or will be under separate cover) forwarded to the Patent and Trademark Office for recording; or

☒ The Assignment recorded on March 25, 1999 at reel 9842, frame 0248.

Pursuant to 37 C.F.R. § 3.73(b) the undersigned assignee hereby states that evidentiary documents have been reviewed and hereby certifies that, to the best of the Assignee's knowledge and belief, title is held by the Assignee.

Direct all telephone calls to N. Kenneth Burraston, (925) 294-4300.

Please change the Attorney Docket Number and correspondence address for the above-identified application to:

Attorney Docket No.: P60-US

FormFactor, Inc.
Legal Department
5666 La Ribera Street
Livermore, CA 94550
(925) 294-4300
(925) 294-8147 fax

Submitted on Behalf of Assignee,

Date: December 12, 2000 By: _____

Stuart L. Merkadeau
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Vice President, Intellectual Property

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